DS05-20883-2E

FLASH MEMORY

CMOS

16M (2M × 8/1M × 16) BIT

MBM29LV160TE/BE -70/90/12

■ GENERAL DESCRIPTION

The MBM29LV160TE/BE is a 16M-bit, 3.0 V-only Flash memory organized as 2M bytes of 8 bits each or 1M words of 16 bits each. The MBM29LV160TE/BE is offered in a 48-pin TSOP (I), 48-pin CSOP and 48-ball FBGA packages. The device is designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard MBM29LV160TE/BE offers access times of 70 ns, 90 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29LV160TE/BE is pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29LV160TE/BE is programmed by executing the program command sequence. This will invoke the Embedded Program™* Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margins. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase™* Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margins.

Any individual sector is typically erased and verified in 1.0 second. (If already preprogrammed.)

within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

(Continued)

■ PRODUCT LINE UP

Part No.		MBM29LV160TE/160BE		
Ordering Part No.	$V_{CC} = 3.3\ V\ ^{+0.3\ V}_{-0.3\ V}$	70	—	—
	$V_{CC} = 3.0\ V\ ^{+0.6\ V}_{-0.3\ V}$	—	90	12
Max. Address Access Time (ns)		70	90	120
Max. $\overline{CE}$ Access Time (ns)		70	90	120
Max. $\overline{OE}$ Access Time (ns)		30	35	50

(Continued)

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29LV160TE/BE is erased when shipped from the factory. The device features single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{\text{BY}}$ output pin. Once the end of a program or erase cycle has been comleted, the device internally resets to the read mode.

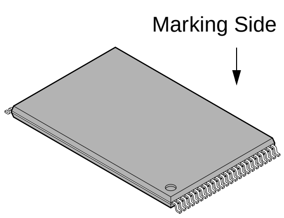
The MBM29LV160TE/BE also has a hardware $\overline{\text{RESET}}$ pin. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm is terminated. The internal state machine is then reset to the read mode. The $\overline{\text{RESET}}$ pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program Algorithm or Embedded Erase Algorithm, the device is automatically reset to the read mode and will have erroneous data stored in the address locations being programmed or erased. These locations need re-writing after the Reset. Resetting the device enables the system's microprocessor to read the boot-up firmware from the Flash memory.

Fujitsu's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29LV160TE/BE memory electrically erases all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

* : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

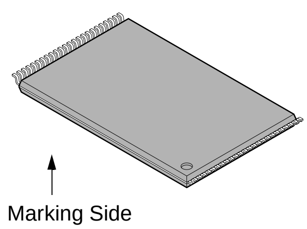
■ PACKAGES

48-pin plastic TSOP (I)



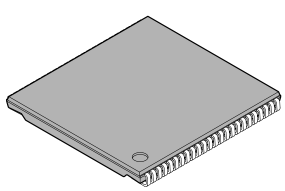
(FPT-48P-M19)

48-pin plastic TSOP (I)



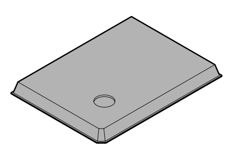
(FPT-48P-M20)

48-pin plastic CSOP



(LCC-48P-M03)

48-pin plastic FBGA



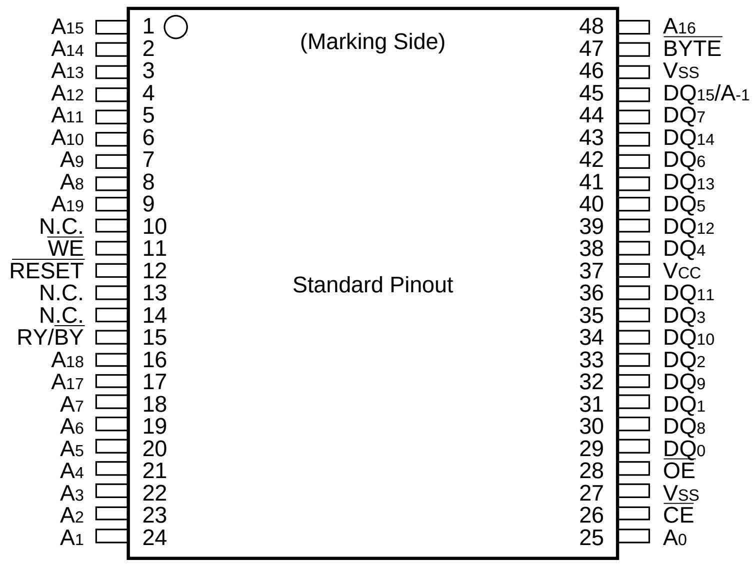
(BGA-48P-M11)

■ FEATURES

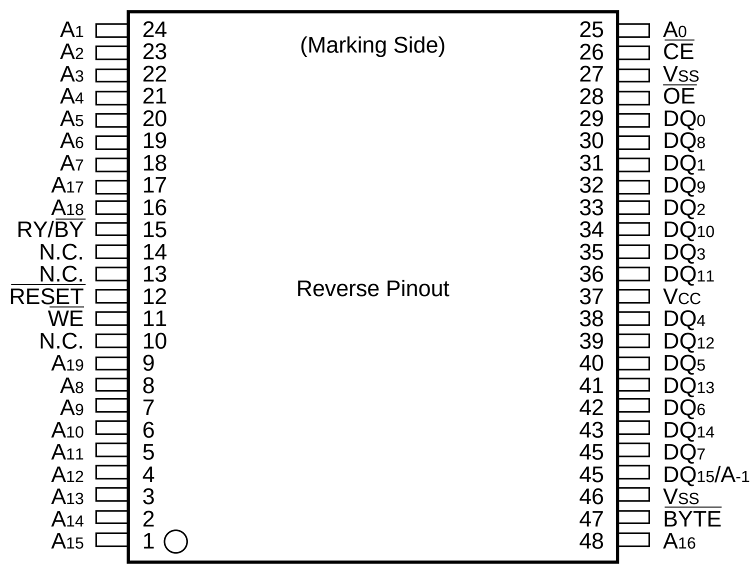
- **0.23 μm Process Technology**
- **Single 3.0 V read, program and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
  48-pin TSOP (I) (Package suffix: TN-Normal Bend Type, TR-Reversed Bend Type)
  48-pin CSOP (Package suffix: PCV)
  48-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  70 ns maximum access time
- **Sector erase architecture**
  One 8K word, two 4K words, one 16K word, and thirty-one 32K words sectors in word mode
  One 16K byte, two 8K bytes, one 32K byte, and thirty-one 64K bytes sectors in byte mode
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switches themselves to low power mode
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector protection**
  Hardware method disables any combination of sectors from program or erase operations
- **Sector Protection Set function by Extended sector Protection command**
- **Fast Programming Function by Extended command**
- **Temporary sector unprotection**
  Temporary sector unprotection via the $\overline{\text{RESET}}$ pin
- **In accordance with CFI (Common Flash Memory Interface)**

■ PIN ASSIGNMENTS

TSOP(I)



(FPT-48P-M19)



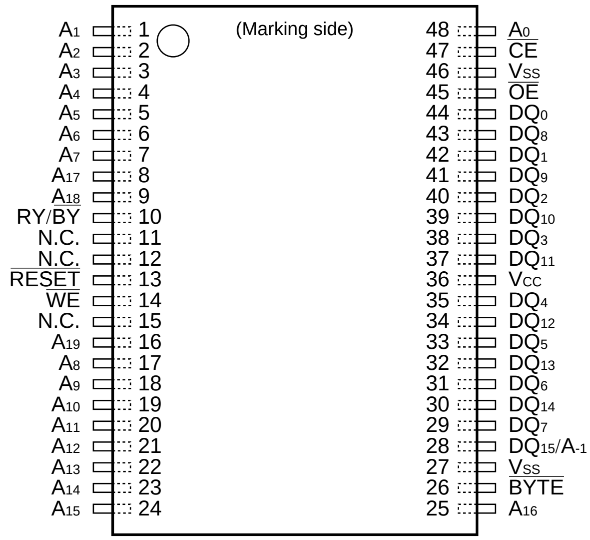
(FPT-48P-M20)

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CSOP

(TOP VIEW)

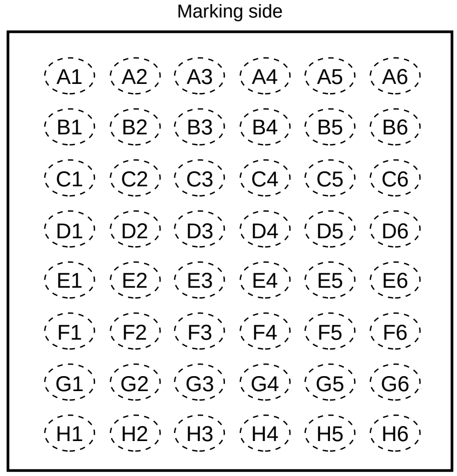


(LCC-48P-M03)

FBGA

(TOP VIEW)

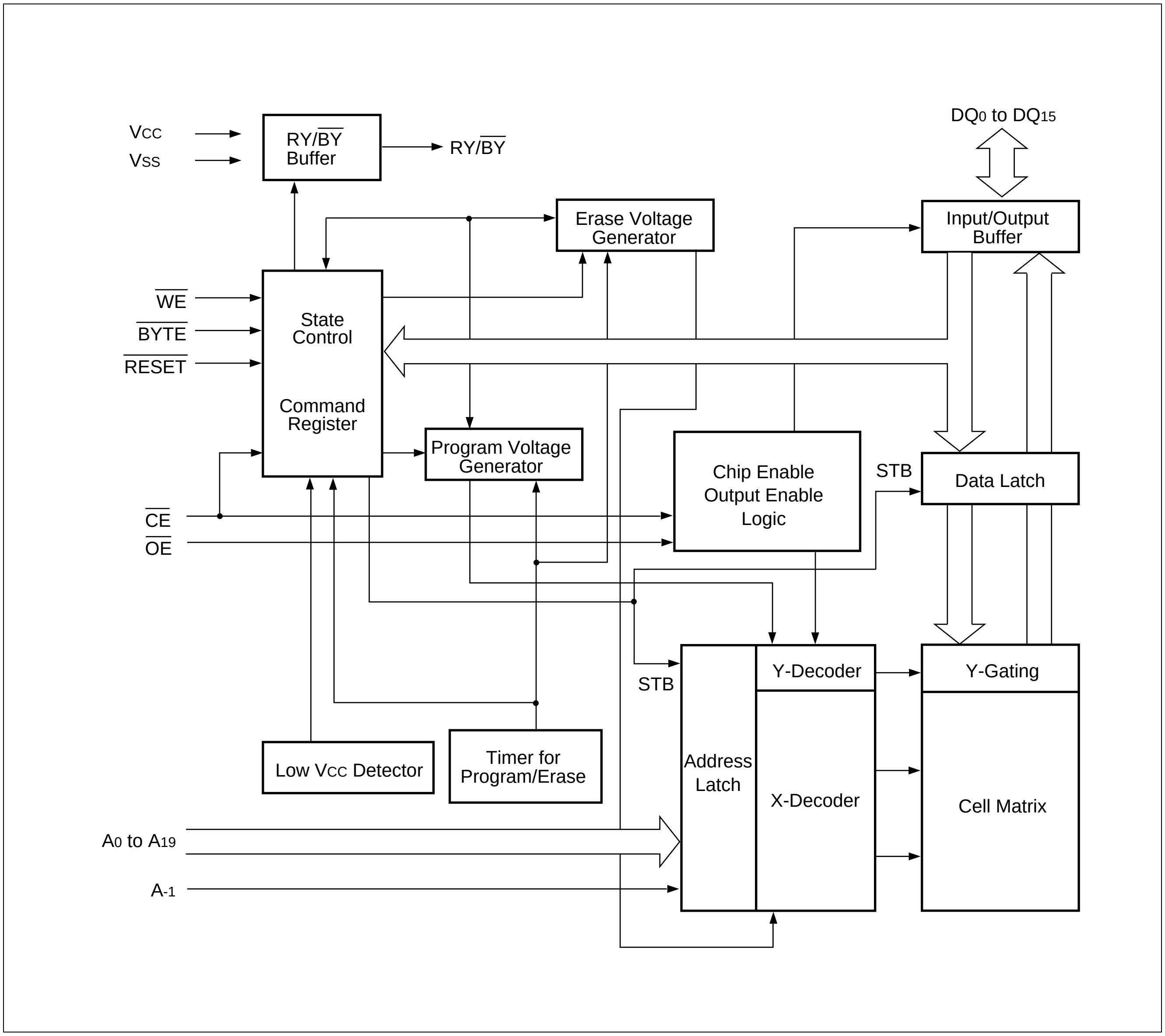
Marking side



(BGA-48P-M11)

A1	A_3	A2	A_7	A3	RY/$\overline{BY}$	A4	$\overline{WE}$	A5	A_9	A6	A_{13}
B1	A_4	B2	A_{17}	B3	N.C.	B4	$\overline{RESET}$	B5	A_8	B6	A_{12}
C1	A_2	C2	A_6	C3	A_{18}	C4	N.C.	C5	A_{10}	C6	A_{14}
D1	A_1	D2	A_5	D3	N.C.	D4	A_{19}	D5	A_{11}	D6	A_{15}
E1	A_0	E2	DQ_0	E3	DQ_2	E4	DQ_5	E5	DQ_7	E6	A_{16}
F1	$\overline{CE}$	F2	DQ_8	F3	DQ_{10}	F4	DQ_{12}	F5	DQ_{14}	F6	$\overline{BYTE}$
G1	$\overline{OE}$	G2	DQ_9	G3	DQ_{11}	G4	V_{CC}	G5	DQ_{13}	G6	DQ_{15}/A_{-1}
H1	V_{SS}	H2	DQ_1	H3	DQ_3	H4	DQ_4	H5	DQ_6	H6	V_{SS}

■ BLOCK DIAGRAM



■ LOGIC SYMBOL

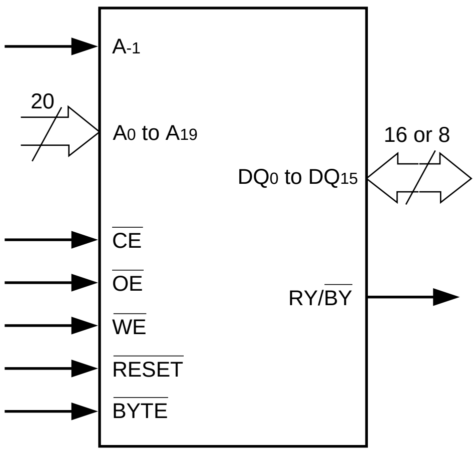


Table 1 MBM29LV160TE/BE Pin Configuration

Pin	Function
A_{-1}, A_0 to A_{19}	Address Inputs
DQ_0 to DQ_{15}	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Pin/ Temporary Sector Unprotection
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
N.C.	Pin Not Connected Internally
V_{SS}	Device Ground
V_{CC}	Device Power Supply

■ DEVICE BUS OPERATIONS

Table 2 MBM29LV160TE/BE User Bus Operation ($\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_0 to DQ_{15}	$\overline{RESET}$
Auto-Select Manufacture Code (1)	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code	H
Read (3)	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	HIGH-Z	H
Output Disable	L	H	H	X	X	X	X	HIGH-Z	H
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection (2), (4)	L	V_{ID}	⊔	L	H	L	V_{ID}	X	H
Verify Sector Protection (2), (4)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection (5)	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)/Standby	X	X	X	X	X	X	X	HIGH-Z	L

Table 3 MBM29LV160TE/BE User Bus Operation ($\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15} / A_{-1}	A_0	A_1	A_6	A_9	DQ_0 to DQ_7	$\overline{RESET}$
Auto-Select Manufacture Code (1)	L	L	H	L	L	L	L	V_{ID}	Code	H
Auto-Select Device Code (1)	L	L	H	L	H	L	L	V_{ID}	Code	H
Read (3)	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	X	HIGH-Z	H
Output Disable	L	H	H	X	X	X	X	X	HIGH-Z	H
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection (2), (4)	L	V_{ID}	⊔	L	L	H	L	V_{ID}	X	H
Verify Sector Protection (2), (4)	L	L	H	L	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection (5)	X	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)/Standby	X	X	X	X	X	X	X	X	HIGH-Z	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. ⊔ = Pulse input. See DC Characteristics for voltage levels.

Notes:
1. Manufacturer and device codes may also be accessed via a command register write sequence. See Table 7.
2. Refer to the section on Sector Protection.
3. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
4. V_{CC} = 3.3 V ±10%
5. It is also used for the extended sector protection.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 8K word, two 4K words, one 16K word, and thirty-one 32K words sectors in word mode.
- One 16K byte, two 8K bytes, one 32K byte, and thirty-one 64K bytes sectors in byte mode.
- Individual-sector, multiple-sector, or bulk-erase capability.
- Individual or multiple-sector protection is user definable.

Sector	Sector Size	(× 8) Address Range	(× 16) Address Range
SA0	64 Kbytes or 32 Kwords	00000H to 0FFFFH	00000H to 07FFFH
SA1	64 Kbytes or 32 Kwords	10000H to 1FFFFH	08000H to 0FFFFH
SA2	64 Kbytes or 32 Kwords	20000H to 2FFFFH	10000H to 17FFFH
SA3	64 Kbytes or 32 Kwords	30000H to 3FFFFH	18000H to 1FFFFH
SA4	64 Kbytes or 32 Kwords	40000H to 4FFFFH	20000H to 27FFFH
SA5	64 Kbytes or 32 Kwords	50000H to 5FFFFH	28000H to 2FFFFH
SA6	64 Kbytes or 32 Kwords	60000H to 6FFFFH	30000H to 37FFFH
SA7	64 Kbytes or 32 Kwords	70000H to 7FFFFH	38000H to 3FFFFH
SA8	64 Kbytes or 32 Kwords	80000H to 8FFFFH	40000H to 47FFFH
SA9	64 Kbytes or 32 Kwords	90000H to 9FFFFH	48000H to 4FFFFH
SA10	64 Kbytes or 32 Kwords	A0000H to AFFFFH	50000H to 57FFFH
SA11	64 Kbytes or 32 Kwords	B0000H to BFFFFH	58000H to 5FFFFH
SA12	64 Kbytes or 32 Kwords	C0000H to CFFFFH	60000H to 67FFFH
SA13	64 Kbytes or 32 Kwords	D0000H to DFFFFH	68000H to 6FFFFH
SA14	64 Kbytes or 32 Kwords	E0000H to EFFFFH	70000H to 77FFFH
SA15	64 Kbytes or 32 Kwords	F0000H to FFFFFH	78000H to 7FFFFH
SA16	64 Kbytes or 32 Kwords	100000H to 10FFFFH	80000H to 87FFFH
SA17	64 Kbytes or 32 Kwords	110000H to 11FFFFH	88000H to 8FFFFH
SA18	64 Kbytes or 32 Kwords	120000H to 12FFFFH	90000H to 97FFFH
SA19	64 Kbytes or 32 Kwords	130000H to 13FFFFH	98000H to 9FFFFH
SA20	64 Kbytes or 32 Kwords	140000H to 14FFFFH	A0000H to A7FFFH
SA21	64 Kbytes or 32 Kwords	150000H to 15FFFFH	A8000H to AFFFFH
SA22	64 Kbytes or 32 Kwords	160000H to 16FFFFH	B0000H to B7FFFH
SA23	64 Kbytes or 32 Kwords	170000H to 17FFFFH	B8000H to BFFFFH
SA24	64 Kbytes or 32 Kwords	180000H to 18FFFFH	C0000H to C7FFFH
SA25	64 Kbytes or 32 Kwords	190000H to 19FFFFH	C8000H to CFFFFH
SA26	64 Kbytes or 32 Kwords	1A0000H to 1AFFFFH	D0000H to D7FFFH
SA27	64 Kbytes or 32 Kwords	1B0000H to 1BFFFFH	D8000H to DFFFFH
SA28	64 Kbytes or 32 Kwords	1C0000H to 1CFFFFH	E0000H to E7FFFH
SA29	64 Kbytes or 32 Kwords	1D0000H to 1DFFFFH	E8000H to EFFFFH
SA30	64 Kbytes or 32 Kwords	1E0000H to 1EFFFFH	F0000H to F7FFFH
SA31	32 Kbytes or 16 Kwords	1F0000H to 1F7FFFH	F8000H to FBFFFH
SA32	8 Kbytes or 4 Kwords	1F8000H to 1F9FFFH	FC000H to FCFFFH
SA33	8 Kbytes or 4 Kwords	1FA000H to 1FBFFFH	FD000H to FDFFFH
SA34	16 Kbytes or 8 Kwords	1FC000H to 1FFFFFH	FE000H to FFFFFH

MBM29LV160TE Top Boot Sector Architecture

Sector	Sector Size	(× 8) Address Range	(× 16) Address Range
SA0	16 Kbytes or 8 Kwords	00000H to 03FFFH	00000H to 01FFFH
SA1	8 Kbytes or 4 Kwords	04000H to 05FFFH	02000H to 02FFFH
SA2	8 Kbytes or 4 Kwords	06000H to 07FFFH	03000H to 03FFFH
SA3	32 Kbytes or 16 Kwords	08000H to 0FFFFH	04000H to 07FFFH
SA4	64 Kbytes or 32 Kwords	10000H to 1FFFFH	08000H to 0FFFFH
SA5	64 Kbytes or 32 Kwords	20000H to 2FFFFH	10000H to 17FFFH
SA6	64 Kbytes or 32 Kwords	30000H to 3FFFFH	18000H to 1FFFFH
SA7	64 Kbytes or 32 Kwords	40000H to 4FFFFH	20000H to 27FFFH
SA8	64 Kbytes or 32 Kwords	50000H to 5FFFFH	28000H to 2FFFFH
SA9	64 Kbytes or 32 Kwords	60000H to 6FFFFH	30000H to 37FFFH
SA10	64 Kbytes or 32 Kwords	70000H to 7FFFFH	38000H to 3FFFFH
SA11	64 Kbytes or 32 Kwords	80000H to 8FFFFH	40000H to 47FFFH
SA12	64 Kbytes or 32 Kwords	90000H to 9FFFFH	48000H to 4FFFFH
SA13	64 Kbytes or 32 Kwords	A0000H to AFFFFH	50000H to 57FFFH
SA14	64 Kbytes or 32 Kwords	B0000H to BFFFFH	58000H to 5FFFFH
SA15	64 Kbytes or 32 Kwords	C0000H to CFFFFH	60000H to 67FFFH
SA16	64 Kbytes or 32 Kwords	D0000H to DFFFFH	68000H to 6FFFFH
SA17	64 Kbytes or 32 Kwords	E0000H to EFFFFH	70000H to 77FFFH
SA18	64 Kbytes or 32 Kwords	F0000H to FFFFFH	78000H to 7FFFFH
SA19	64 Kbytes or 32 Kwords	100000H to 10FFFFH	80000H to 87FFFH
SA20	64 Kbytes or 32 Kwords	110000H to 11FFFFH	88000H to 8FFFFH
SA21	64 Kbytes or 32 Kwords	120000H to 12FFFFH	90000H to 97FFFH
SA22	64 Kbytes or 32 Kwords	130000H to 13FFFFH	98000H to 9FFFFH
SA23	64 Kbytes or 32 Kwords	140000H to 14FFFFH	A0000H to A7FFFH
SA24	64 Kbytes or 32 Kwords	150000H to 15FFFFH	A8000H to AFFFFH
SA25	64 Kbytes or 32 Kwords	160000H to 16FFFFH	B0000H to B7FFFH
SA26	64 Kbytes or 32 Kwords	170000H to 17FFFFH	B8000H to BFFFFH
SA27	64 Kbytes or 32 Kwords	180000H to 18FFFFH	C0000H to C7FFFH
SA28	64 Kbytes or 32 Kwords	190000H to 19FFFFH	C8000H to CFFFFH
SA29	64 Kbytes or 32 Kwords	1A0000H to 1AFFFFH	D0000H to D7FFFH
SA30	64 Kbytes or 32 Kwords	1B0000H to 1BFFFFH	D8000H to DFFFFH
SA31	64 Kbytes or 32 Kwords	1C0000H to 1CFFFFH	E0000H to E7FFFH
SA32	64 Kbytes or 32 Kwords	1D0000H to 1DFFFFH	E8000H to EFFFFH
SA33	64 Kbytes or 32 Kwords	1E0000H to 1EFFFFH	F0000H to F7FFFH
SA34	64 Kbytes or 32 Kwords	1F0000H to 1FFFFFH	F8000H to FFFFFH

MBM29LV160BE Bottom Boot Sector Architecture

■ FUNCTIONAL DESCRIPTION

• Read Mode

The MBM29LV160TE/BE has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.
Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least t_{ACC} - t_{OE} time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from "H" or "L".

• Standby Mode

There are two ways to implement the standby mode on the MBM29LV160TE/BE devices. One is by using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.
When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at V_{CC} ±0.3 V. Under this condition the current consumed is less than 5 μA max. During Embedded Algorithm operation, V_{CC} Active current (I_{CC2}) is required even $\overline{CE}$ = "H". The device can be read with standard access time (t_{CE}) from either of these standby modes.
When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with the $\overline{RESET}$ input held at V_{SS} ±0.3 V ($\overline{CE}$ = "H" or "L"). Under this condition the current consumed is less than 5 μA max. Once the $\overline{RESET}$ pin is taken high, the device requires t_{RH} of wake up time before outputs are valid for read access.
In the standby mode, the outputs are in the high-impedance state, independent of the $\overline{OE}$ input.

• Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29LV160TE/BE data. This mode can be used effectively with an application requesting low power consumption such as handy terminals.
To activate this mode, MBM29LV160TE/BE automatically switches itself to low power mode when addresses remain stable for 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ in this mode. During such mode, the current consumed is typically 1 μA (CMOS Level).
Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

• Output Disable

If the $\overline{OE}$ input is at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high-impedance state.

• Autoselect

The Autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. The intent is to allow programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The Autoselect command may also be used to check the status of write-protected sectors. (See Tables 4.1 and 4.2.) This mode is functional over the entire temperature range of the device.
To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON'T CARES except A_0, A_1, and A_6 (A_{-1}). (See Table 2 or Table 3.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29LV160TE/BE is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 7, Command Definitions.

Byte 0 ($A_0 = V_{IL}$) represents the manufacture's code and byte 1 ($A_0 = V_{IH}$) represents the device identifier code. For the MBM29LV160TE/BE these two bytes are given in the Table 4.2. All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A_1 must be V_{IL}. (See Tables 2 or 3.) For device indentification in word mode ($\overline{BYTE} = V_{IH}$), DQ_9 and DQ_{13} are equal to '1' and DQ_8, DQ_{10} to DQ_{12}, DQ_{14}, and DQ_{15} are equal to '0'.

If $\overline{BYTE} = V_{IL}$ (for byte mode), the device code is C4H (for top boot block) or 49H (for bottom boot block). If $\overline{BYTE} = V_{IH}$ (for word mode), the device code is 22C4H (for top boot block) or 2249H (for bottom boot block).

In order to determine which sectors are write protected, A_1 must be at V_{IH} while running through the sector addresses; if the selected sector is protected, a logical '1' will be output on DQ_0 (DQ_0 =1).

Table 4.1 MBM29LV160TE/BE Sector Protection Verify Autoselect Code

Type			A_{12} to A_{19}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04H
Device Code	MBM29LV160TE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	C4H
		Word					X	22C4H
	MBM29LV160BE	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	49H
		Word					X	2249H
Sector Protection			Sector Addresses	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01H*2

*1: A_{-1} is for Byte mode.

*2: Outputs 01H at protected sector addresses and outputs 00H at unprotected sector addresses.

Table 4.2 Expanded Autoselect Code Table

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacture's Code			04H	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29LV160TE	(B)	C4H	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1	1	0	0	0	1	0	0
		(W)	22C4H	0	0	1	0	0	0	1	0	1	1	0	0	0	1	0	0
	MBM29LV160BE	(B)	49H	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	1	0	0	1	0	0	1
		(W)	2249H	0	0	1	0	0	0	1	0	0	1	0	0	1	0	0	1
Sector Protection			01H	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode
(W): Word mode

Table 5 Sector Address Tables (MBM29LV160TE)

Sector Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	(× 8) Address Range	(× 16) Address Range
SA0	0	0	0	0	0	X	X	X	00000H to 0FFFFH	00000H to 07FFFH
SA1	0	0	0	0	1	X	X	X	10000H to 1FFFFH	08000H to 0FFFFH
SA2	0	0	0	1	0	X	X	X	20000H to 2FFFFH	10000H to 17FFFH
SA3	0	0	0	1	1	X	X	X	30000H to 3FFFFH	18000H to 1FFFFH
SA4	0	0	1	0	0	X	X	X	40000H to 4FFFFH	20000H to 27FFFH
SA5	0	0	1	0	1	X	X	X	50000H to 5FFFFH	28000H to 2FFFFH
SA6	0	0	1	1	0	X	X	X	60000H to 6FFFFH	30000H to 37FFFH
SA7	0	0	1	1	1	X	X	X	70000H to 7FFFFH	38000H to 3FFFFH
SA8	0	1	0	0	0	X	X	X	80000H to 8FFFFH	40000H to 47FFFH
SA9	0	1	0	0	1	X	X	X	90000H to 9FFFFH	48000H to 4FFFFH
SA10	0	1	0	1	0	X	X	X	A0000H to AFFFFH	50000H to 57FFFH
SA11	0	1	0	1	1	X	X	X	B0000H to BFFFFH	58000H to 5FFFFH
SA12	0	1	1	0	0	X	X	X	C0000H to CFFFFH	60000H to 67FFFH
SA13	0	1	1	0	1	X	X	X	D0000H to DFFFFH	68000H to 6FFFFH
SA14	0	1	1	1	0	X	X	X	E0000H to EFFFFH	70000H to 77FFFH
SA15	0	1	1	1	1	X	X	X	F0000H to FFFFFH	78000H to 7FFFFH
SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	80000H to 87FFFH
SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	88000H to 8FFFFH
SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	90000H to 97FFFH
SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	98000H to 9FFFFH
SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	A0000H to A7FFFH
SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	A8000H to AFFFFH
SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	B0000H to B7FFFH
SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	B8000H to BFFFFH
SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	C0000H to C7FFFH
SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	C8000H to CFFFFH
SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	D0000H to D7FFFH
SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	D8000H to DFFFFH
SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	E0000H to E7FFFH
SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	E8000H to EFFFFH
SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	F0000H to F7FFFH
SA31	1	1	1	1	1	0	X	X	1F0000H to 1F7FFFH	F8000H to FBFFFH
SA32	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	FC000H to FCFFFH
SA33	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	FD000H to FDFFFH
SA34	1	1	1	1	1	1	1	X	1FC000H to 1FFFFFH	FE000H to FEFFFH

Table 6 Sector Address Tables (MBM29LV160BE)

Sector Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	(× 8) Address Range	(× 16) Address Range
SA0	0	0	0	0	0	0	0	X	00000H to 03FFFH	00000H to 01FFFH
SA1	0	0	0	0	0	0	1	0	04000H to 05FFFH	02000H to 02FFFH
SA2	0	0	0	0	0	0	1	1	06000H to 07FFFH	03000H to 03FFFH
SA3	0	0	0	0	0	1	0	X	08000H to 0FFFFH	04000H to 07FFFH
SA4	0	0	0	0	1	X	X	X	10000H to 1FFFFH	08000H to 0FFFFH
SA5	0	0	0	1	0	X	X	X	20000H to 2FFFFH	10000H to 17FFFH
SA6	0	0	0	1	1	X	X	X	30000H to 3FFFFH	18000H to 1FFFFH
SA7	0	0	1	0	0	X	X	X	40000H to 4FFFFH	20000H to 27FFFH
SA8	0	0	1	0	1	X	X	X	50000H to 5FFFFH	28000H to 2FFFFH
SA9	0	0	1	1	0	X	X	X	60000H to 6FFFFH	30000H to 37FFFH
SA10	0	0	1	1	1	X	X	X	70000H to 7FFFFH	38000H to 3FFFFH
SA11	0	1	0	0	0	X	X	X	80000H to 8FFFFH	40000H to 47FFFH
SA12	0	1	0	0	1	X	X	X	90000H to 9FFFFH	48000H to 4FFFFH
SA13	0	1	0	1	0	X	X	X	A0000H to AFFFFH	50000H to 57FFFH
SA14	0	1	0	1	1	X	X	X	B0000H to BFFFFH	58000H to 5FFFFH
SA15	0	1	1	0	0	X	X	X	C0000H to CFFFFH	60000H to 67FFFH
SA16	0	1	1	0	1	X	X	X	D0000H to DFFFFH	68000H to 6FFFFH
SA17	0	1	1	1	0	X	X	X	E0000H to EFFFFH	70000H to 77FFFH
SA18	0	1	1	1	1	X	X	X	F0000H to FFFFFH	78000H to 7FFFFH
SA19	1	0	0	0	0	X	X	X	100000H to 1FFFFFH	80000H to 87FFFH
SA20	1	0	0	0	1	X	X	X	110000H to 11FFFFH	88000H to 8FFFFH
SA21	1	0	0	1	0	X	X	X	120000H to 12FFFFH	90000H to 97FFFH
SA22	1	0	0	1	1	X	X	X	130000H to 13FFFFH	98000H to 9FFFFH
SA23	1	0	1	0	0	X	X	X	140000H to 14FFFFH	A0000H to A7FFFH
SA24	1	0	1	0	1	X	X	X	150000H to 15FFFFH	A8000H to 8FFFFH
SA25	1	0	1	1	0	X	X	X	160000H to 16FFFFH	B0000H to B7FFFH
SA26	1	0	1	1	1	X	X	X	170000H to 17FFFFH	B8000H to BFFFFH
SA27	1	1	0	0	0	X	X	X	180000H to 18FFFFH	C0000H to C7FFFH
SA28	1	1	0	0	1	X	X	X	190000H to 19FFFFH	C8000H to CFFFFH
SA29	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	D0000H to D7FFFH
SA30	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	D8000H to DFFFFH
SA31	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	E0000H to E7FFFH
SA32	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	E8000H to EFFFFH
SA33	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	F0000H to F7FFFH
SA34	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFH	F8000H to FFFFFH

• Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.
The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.
Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

• Sector Protection

The MBM29LV160TE/BE features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 34). The sector protection feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected.
To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, $\overline{CE}$ = V_{IL}, A_0 = A_6 = V_{IL}, A_1 = V_{IH}. The sector addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. Tables 5 and 6 define the sector address for each of the thirty five (35) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See Figures 17 and 24 for sector protection waveforms and algorithm.
To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector. Otherwise the device will read 00H for an unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON'T CARES. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes. A_{-1} requires to V_{IL} in byte mode.
It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) represents the sector address will produce a logical "1" at DQ_0 for a protected sector. See Tables 4.1 and 4.2 for Autoselect codes.

• Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the MBM29LV160TE/BE devices in order to change data. The Sector Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again. (See Figures 18 and 25.)

Table 7 MBM29LV160TE/BE Standard Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	Word	1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Autoselect	Word	3	555H	AAH	2AAH	55H	555H	90H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Erase Suspend		1	XXXH	B0H	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	XXXH	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Fast Program *1	Word	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXH											
Reset from Fast Mode *1	Word	2	XXXH	90H	XXXH	*4 F0H	—	—	—	—	—	—	—	—
	Byte		XXXH		XXXH									
Extended Sector Protection *2	Word	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
	Byte													
Query *3	Word	1	55H	98H	—	—	—	—	—	—	—	—	—	—
	Byte		AAH											

Notes: 1. Address bits A_{11} to A_{19} = X = "H" or "L" for all address commands except or Program Address (PA) and Sector Address (SA).

2. Bus operations are defined in Tables 2 and 3.

3. RA =Address of the memory location to be read.
   PA =Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA =Address of the sector to be erased. The combination of A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.

4. RD =Data read from location RA during read operation.
   PD =Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.

5. SPA =Sector address to be protected. Set sector address (SA) and (A_6, A_1, A_0) = (0, 1, 0).
   SD =Sector protection verify data. Output 01H at protected sector addressed and output 00H at unprotected sector addresses.

6. The system should generate the following address patterns:
   Word Mode: 555H or 2AAH to addresses A_0 to A_{10}
   Byte Mode: AAAH or 555H to addresses A_{-1} to A_{10}

7. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

*1: This command is valid while Fast Mode.

*2: This command is valid while $\overline{RESET}$ = V_{ID}.

*3: The valid addresses are A_6 to A_0. The other addresses are "Don't care".

*4: The data "00H" is also acceptable.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in an improper sequence will reset the device to the read mode. Table 7 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_0 to DQ_7 and DQ_8 to DQ_{15} bits are ignored.

• Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to read mode, the read/reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory contents occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters. (See Figure 5.1.)

• Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufactures and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register. Following the last command write, a read cycle from address XX00H retrieves the manufacture code of 04H. A read cycle from address XX01H for ×16 (XX02H for ×8) retrieves the device code (MBM29LV160TE = C4H and MBM29LV160BE = 49H for ×8 mode; MBM29LV160TE = 22C4H and MBM29LV160BE = 2249H for ×16 mode). (See Tables 4.1 and 4.2.)

All manufactures and device codes will exhibit odd parity with DQ_7 defined as the parity bit.

The sector state (protection or unprotection) will be indicated by address XX02H for ×16 (XX04H for ×8).

Scanning the sector addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” at device output DQ_0 for a protected sector. The programming verification should be perform margin mode verification on the protected sector. (See Tables 2 and 3.)

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register and, also to write the Autoselect command during the operation, by executing it after writing the Read/Reset command sequence.

• Byte/Word Programming

The device is programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of the last $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. (See Figures 6 and 7.)

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the device return to the read mode and addresses are no longer latched. (See Table 8, Hardware Sequence Flags.) Therefore, the device requires that a valid address be supplied by the system at this time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If hardware reset occures during the programming operation, it is impossible to guarantee whether the data being written is correct or not.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from read/reset mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.
Figure 20 illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

• Chip Erase

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.
Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. (Preprogram Function.) The system is not required to provide any controls or timings during these operations.
The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ_7 is "1" (See Write Operation Status section.) at which time the device returns to read mode. (See Figure 8.)
Figure 21 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

• Sector Erase

Sector erase is a six-bus cycle operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (Data = 30H) is latched on the rising edge of $\overline{WE}$. After a time-out of "t_{TOW}" from the rising edge of the last sector erase command, the sector erase operation will begin.
Multiple sectors may be erased concurrently by writing six-bus cycle operations on Table 7. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than "t_{TOW}" otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of "t_{TOW}" from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the "t_{TOW}" time-out window the timer is reset. Monitor DQ_3 to determine if the sector erase timer window is still open. (See section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once excution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 34).
Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram Function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.
The automatic sector erase begins after the "t_{TOW}" time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ_7 is "1" (See Write Operation Status section) at which time the device returns to the read mode. $\overline{Data}$ polling must be performed at an address within any of the sectors being erased. Multiple Sector Erase Time; [Sector Program Time (Preprogramming) + Sector Erase Time] $\times$ Number of Sector Erase.
Figure 21 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

• Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or program to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if

written during the Chip Erase operation or Embedded Program Algorithm. Writting the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command resumes the erase operation. The addresses are “DON’T CARES” when writing the Erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “t_{SPD}” to suspend the erase operation. When the devices have entered the erase-suspended mode, the RY/$\overline{BY}$ output pin and the DQ_7 bit will be at logic “1”, and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This Program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the RY/$\overline{BY}$ output pin, $\overline{\text{Data}}$ polling of DQ_7, or the Toggle Bit (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

• Extended Command

(1) Fast Mode

MBM29LV160TE/BE has Fast Mode function. This mode dispenses with the initial two unlock cycles required in the standard program command sequence writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. (Refer to the Figure 26 Extended algorithm.) The V_{CC} active current is required even $\overline{CE}$ = V_{IH} during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0H) and data write cycles (PA/PD). (Refer to the Figure 26 Extended algorithm.)

(3) Extended Sector Protection

In addition to normal sector protection, the MBM29LV160TE/BE has Extended Sector Protection as extended function. This function enable to protect sector by forcing V_{ID} on $\overline{RESET}$ pin and write a commnad sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector protection in this mode. The extended sector protect requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60H) into the command register. Then, the sector addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector to be protected (recommend to set V_{IL} for the other addresses pins), and write extended sector protect command (60H). A sector is typically protected in 250 µs. To verify programming of the protection circuitry, the sector addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40H). Following the command write, a logical “1” at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical “0”, please repeat to write extended sector protect command (60H) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH}.

(4) CFI (Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98H) into the command register. Following the command write, a read cycle from specific address retrives device information. Please note that output data of upper byte (DQ_8 to DQ_{15}) is “0” in word mode (16 bit) read. Refer to the CFI code table. To terminate operation, it is necessary to write the read/reset command sequence into the register.

• Write Operation Status

Table 8 Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded/Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspend Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle (Note 1)	0	0	1 (Note 2)
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded/Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspend Program (Non-Erase Suspended Sector)		$\overline{DQ_7}$	Toggle	1	0	N/A

Notes: 1. Performing successive read operations from any address will cause DQ_6 to toggle.
2. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.
3. DQ_0 and DQ_1 are reserve pins for future use.
4. DQ_4 is Fujitsu internal use only.

• DQ_7

$\overline{\text{Data}}$ Polling

The MBM29LV160TE/BE device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the devices will produce the complement of the data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ_7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in Figure 22.

For chip erase and sector erase, $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six-write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at a sector address within any of the sectors being erased and not at a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the MBM29LV160TE/BE data pins (DQ_7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ_7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Program Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out.

See Figure 9 for the $\overline{\text{Data}}$ Polling timing specifications and diagram.

- **DQ_6**

Toggle Bit I

The MBM29LV160TE/BE also feature the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.
During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the device will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data can be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six-write pulse sequence. The Toggle Bit I is active during the sector time out.
In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 μs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the Toggle Bit I for about 200 μs and then drop back into read mode, having changed none of the data.
Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause the DQ_6 to toggle.
See Figure 10 and Figure 23 for the Toggle Bit I timing specifications and diagram.

- **DQ_5**

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Tables 2 and 3.
The DQ_5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 and DQ_6 never stops toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device with command sequence.

- **DQ_3**

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{Data}$ Polling and Toggle Bit I are valid after the initial sector erase command sequence.
If $\overline{Data}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{Data}$ Polling or Toggle Bit I. If DQ_3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent sector erase command. If DQ_3 is high on the second status check, the command may not have been accepted.
See Table 8: Hardware Sequence Flags.

- **DQ_2**

Toggle Bit II

This Toggle Bit II, along with DQ_6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.
Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic "1" at DQ_2.
DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress.
For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also Table 9 and Figure 11.
Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Table 9 Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle
Erase Suspend Read (Erase Suspended Sector) (Note 1)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle (Note 1)	1 (Note 2)

Notes: 1. Performing successive read operations from any address will cause DQ_6 to toggle.
2. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.

- **RY/$\overline{\text{BY}}$**

Ready/Busy Pin

The MBM29LV160TE/BE provides a RY/$\overline{\text{BY}}$ open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/$\overline{\text{BY}}$ pin is low, the devices will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the MBM29LV160TE/BE is placed in an Erase Suspend mode, the RY/$\overline{\text{BY}}$ output will be high, by means of connecting with a pull-up resister to V_{CC}.
During programming, the RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the fourth $\overline{\text{WE}}$ pulse. During an erase operation, the RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the sixth $\overline{\text{WE}}$ pulse. The RY/$\overline{\text{BY}}$ pin will indicate a busy condition during the $\overline{\text{RESET}}$ pulse. See Figures 12 and 13 for a detailed timing diagram. The RY/$\overline{\text{BY}}$ pin is pulled high in standby mode.
Since this is an open-drain output, RY/$\overline{\text{BY}}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

- **$\overline{\text{RESET}}$**

Hardware Reset Pin

The MBM29LV160TE/BE device may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL}. The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least "t_{RP}" in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode "t_{READY}" after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the device requires an additional "t_{RH}" before it allows read access. When the $\overline{\text{RESET}}$ pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{\text{BY}}$ output signal should be ignored during the $\overline{\text{RESET}}$ pulse. Refer to Figure 13 for the timing diagram. Refer to Temporary Sector Unprotection for additional functionality.
If hardware reset occurs during Embedded Erase Algorithm, there is a possibility that the erasing sector(s) will need to be erased again before they can be programmed.

- **Byte/Word Configuration**

The $\overline{\text{BYTE}}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the MBM29LV160TE/BE device. When this pin is driven high, the device operates in the word (16-bit) mode. The data is read and programmed at DQ_0 to DQ_{15}. When this pin is driven low, the device operates in byte (8-bit) mode. Under this mode, DQ_{15}/A_{-1} pin becomes the lowest address bit and DQ_8 to DQ_{14} bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_0 to DQ_7 and DQ_8 to DQ_{15} bits are ignored. Refer to Figures 14, 15 and 16 for the timing diagram.

- **Data Protection**

The MBM29LV160TE/BE is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine to the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequence.
The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

- **Low V_{CC} Write Inhibit**

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO} (min.). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO} (min.).
If the Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) will need to be erased again prior to programming.

- **Write Pulse "Glitch" Protection**

Noise pulses of less than 5 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$, or $\overline{\text{WE}}$ will not change the command registers.

- **Logical Inhibit**

Writing is inhibited by holding any one of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{WE}} = V_{IH}$. To initiate a write, $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

- **Power-up Write Inhibit**

Power-up of the devices with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to read mode on power-up.

Table 10 Common Flash Memory Interface Code

Description	A_0 to A_6	DQ_0 to DQ_{15}
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h
Primary OEM Command Set 2h: AMD/FJ standard type	13h 14h	0002h 0000h
Address for Primary Extended Table	15h 16h	0040h 0000h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h
V_{CC} Min. (write/erase) D7-4: volt, D3-0: 100 mvolt	1Bh	0027h
V_{CC} Max. (write/erase) D7-4: volt, D3-0: 100 mvolt	1Ch	0036h
V_{PP} Min. voltage	1Dh	0000h
V_{PP} Max. voltage	1Eh	0000h
Typical timeout per single byte/word write 2^N µs	1Fh	0004h
Typical timeout for Min. size buffer write 2^N µs	20h	0000h
Typical timeout per individual block erase 2^N ms	21h	000Ah
Typical timeout for full chip erase 2^N ms	22h	0000h
Max. timeout for byte/word write 2^N times typical	23h	0005h
Max. timeout for buffer write 2^N times typical	24h	0000h
Max. timeout per individual block erase 2^N times typical	25h	0004h
Max. timeout for full chip erase 2^N times typical	26h	0000h
Device Size = 2^N byte	27h	0015h
Flash Device Interface description	28h 29h	0002h 0000h
Max. number of byte in multi-byte write = 2^N	2Ah 2Bh	0000h 0000h
Number of Erase Block Regions within device	2Ch	0004h

Description	A_0 to A_6	DQ_0 to DQ_{15}
Erase Block Region 1 Information	2Dh 2Eh 2Fh 30h	0000h 0000h 0040h 0000h
Erase Block Region 2 Information	31h 32h 33h 34h	0001h 0000h 0020h 0000h
Erase Block Region 3 Information	35h 36h 37h 38h	0000h 0000h 0080h 0000h
Erase Block Region 4 Information	39h 3Ah 3Bh 3Ch	001Eh 0000h 0000h 0001h
Query-unique ASCII string "PRI"	40h 41h 42h	0050h 0052h 0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0031h
Address Sensitive Unlock 0 = Required 1 = Not Required	45h	0000h
Erase Suspend 0 = Not Supported 1 = To Read Only 2 = To Read & Write	46h	0002h
Sector Protect 0 = Not Supported X = Number of sectors in per group	47h	0001h
Sector Temporary Unprotect 00 = Not Supported 01 = Supported	48h	0001h
Sector Protection Algorithm	49h	04h
Number of Sector for Bank 2 00h = Not Supported	4Ah	00h
Burst Mode Type 00h = Not Supported	4Bh	00h
Page Mode Type 00h = Not Supported	4Ch	00h

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, $\overline{RESET}$ (Note 1)	V_{IN}, V_{OUT}	–0.5	V_{CC}+0.5	V
Power Supply Voltage (Note 1)	V_{CC}	–0.5	+5.5	V
A_9, $\overline{OE}$, and $\overline{RESET}$ (Note 2)	V_{IN}	–0.5	+13.0	V

Notes: 1. Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are V_{CC} +0.5 V. During voltage transitions,outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on A_9, $\overline{OE}$, and $\overline{RESET}$ pins are –0.5 V. During voltage transitions, A_9, $\overline{OE}$, and $\overline{RESET}$ pins may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9, $\overline{OE}$, and $\overline{RESET}$ pins are +13.0 V which may positive overshoot to 14.0 V for periods of up to 20 ns. Voltage difference between input voltage and supply voltage (V_{IN} – V_{CC}) do not exceed 9 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Ambient Temperature	(-70)	T_A	–20	—	+70	°C
	(-90/12)		–40	—	+85	°C
Power Supply Voltage	(-70)	V_{CC}	+3.0	—	+3.6	V
	(-90/12)		+2.7	—	+3.6	V

Operating ranges define those limits between which the functionality of the device is quaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT

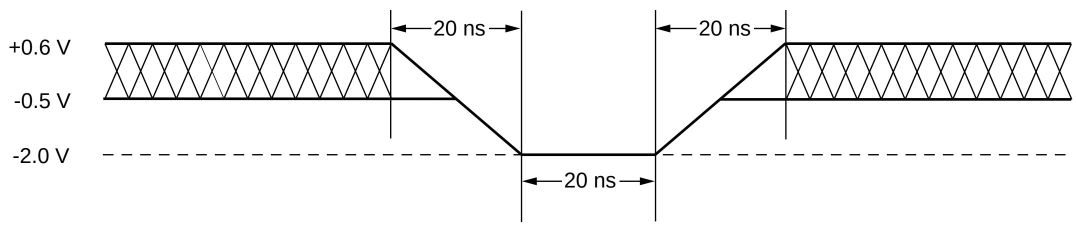


Figure 1 Maximum Negative Overshoot Waveform

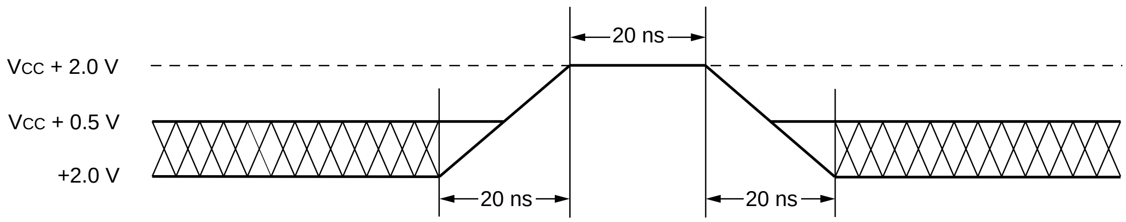
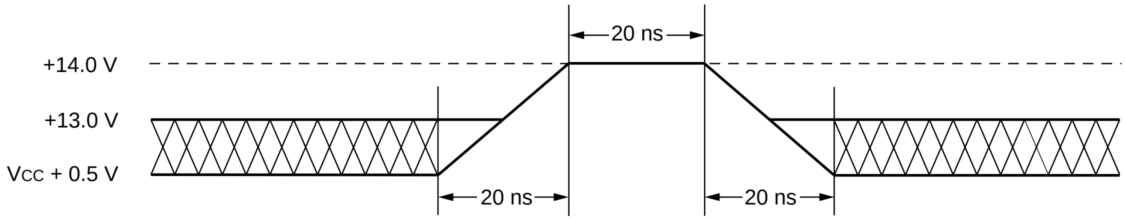


Figure 2 Maximum Positive Overshoot Waveform 1



Note : This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Figure 3 Maximum Positive Overshoot Waveform 2

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.		–1.0	+1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max.		–1.0	+1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	$V_{CC} = V_{CC}$ Max., A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	35	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ f = 10 MHz	Byte	—	30	mA
			Word		35	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ f = 5 MHz	Byte	—	15	mA
			Word		17	
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	35	mA
I_{CC3}	V_{CC} Current (Standby)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V		—	5	µA
I_{CC4}	V_{CC} Current (Standby, $\overline{RESET}$)	$V_{CC} = V_{CC}$ Max., $\overline{RESET} = V_{SS} \pm 0.3$ V		—	5	µA
I_{CC5}	V_{CC} Current (Automatic Sleep Mode) (Note 3)	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V, $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V		—	5	µA
V_{IL}	Input Low Level	—		–0.5	0.6	V
V_{IH}	Input High Level	—		2.0	V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect, Sector Protection, and Temporary Sector Unprotection (A_9, $\overline{OE}$, $\overline{RESET}$) (Note 4)	—		11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 4.0 mA, $V_{CC} = V_{CC}$ Min.		—	0.45	V
V_{OH1}	Output High Voltage Level	I_{OH} = –2.0 mA, $V_{CC} = V_{CC}$ Min.		2.4	—	V
V_{OH2}		I_{OH} = –100 µA		V_{CC} – 0.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage	—		2.3	2.5	V

Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
2. I_{CC} active while Embedded Erase or Embedded Program is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
4. (V_{ID} – V_{CC}) do not exceed 9 V.

2. AC Characteristics

- **Read Only Operations Characteristics**

Parameter Symbols		Description	Test Setup		70 (Note)	90 (Note)	12 (Note)	Unit
JEDEC	Standard							
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output HIGH-Z	—	Max.	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output HIGH-Z	—	Max.	25	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	Min.	0	0	0	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	Max.	20	20	20	µs
—	t_{ELFL} t_{ELFH}	$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	Max.	5	5	5	ns

Note : Test Conditions:
Output Load:1 TTL gate and 30 pF (MBM29LV160TD/BD-70)
1 TTL gate and 100 pF (MBM29LV160TD/BD-90/12)
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output:1.5 V

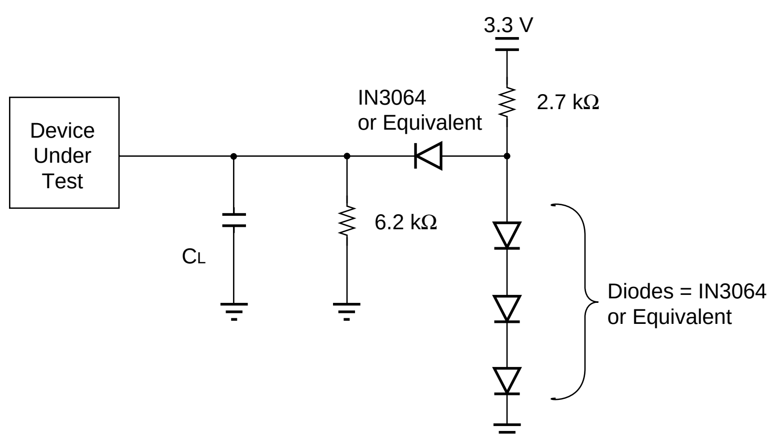


Figure 4 Test Conditions

- **Write (Erase/Program) Operations**

Parameter Symbols: JEDEC	Parameter Symbols: Standard	Description			70	90	12	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	0	0	ns
—	t_{OES}	Output Enable Setup Time		Min.	0	0	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling	Min.	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{\text{OE}}$ High to $\overline{\text{CE}}$ Low)		Min.	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{\text{CE}}$ Setup Time		Min.	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{\text{WE}}$ Setup Time		Min.	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{\text{CE}}$ Hold Time		Min.	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{\text{WE}}$ Hold Time		Min.	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	35	45	50	ns
t_{ELEH}	t_{CP}	$\overline{\text{CE}}$ Pulse Width		Min.	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	25	25	30	ns
t_{EHEL}	t_{CPH}	$\overline{\text{CE}}$ Pulse Width High		Min.	25	25	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Byte	Typ.	8	8	8	µs
			Word		16	16	16	
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ.	1	1	1	s
—	t_{VCS}	V_{CC} Setup Time		Min.	50	50	50	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)		Min.	500	500	500	ns
—	t_{VLHT}	Voltage Transition Time (Note 2)		Min.	4	4	4	µs
—	t_{WPP}	Write Pulse Width (Note 2)		Min.	100	100	100	µs
—	t_{OESP}	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active (Note 2)		Min.	4	4	4	µs
—	t_{CSP}	$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active (Note 2)		Min.	4	4	4	µs
—	t_{RB}	Recover Time From RY/$\overline{\text{BY}}$		Min.	0	0	0	ns

(Continued)

(Continued)

Parameter Symbols		Description		70	90	12	Unit
JEDEC	Standard						
—	t_{RP}	$\overline{RESET}$ Pulse Width	Min.	500	500	500	ns
—	t_{RH}	$\overline{RESET}$ High Level Period Before Read	Min.	200	200	200	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	Max.	90	90	90	ns
—	t_{EOE}	Delay Time from Embedded Output Enable	Max.	70	90	120	ns
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output HIGH-Z	Max.	30	35	50	ns
—	t_{FHQV}	$\overline{BYTE}$ Switching High to Output Active	Min.	30	35	50	ns
—	t_{TOW}	Erase Time-out Time	Min.	50	50	50	µs
—	t_{SPD}	Erase Suspend Transition Time	Max.	20	20	20	µs

Notes: 1. This does not include the preprogramming time.

2. This timing is for Sector Protection operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Byte Programming Time	—	8	300	µs	Excludes system-level overhead
Word Programming Time	—	16	360		
Chip Programming Time	—	16.8	50	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

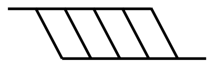
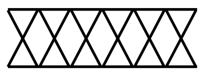
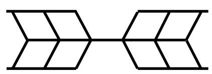
■ PIN CAPACITANCE

Parameter	Symbol	Test Setup	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$	6	7.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8	10	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	7.5	9	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ TIMING DIAGRAM

• **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Change from H to L
	May Change from L to H	Will Be Change from L to H
	“H” or “L”; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line Is High-Impedance “Off” State

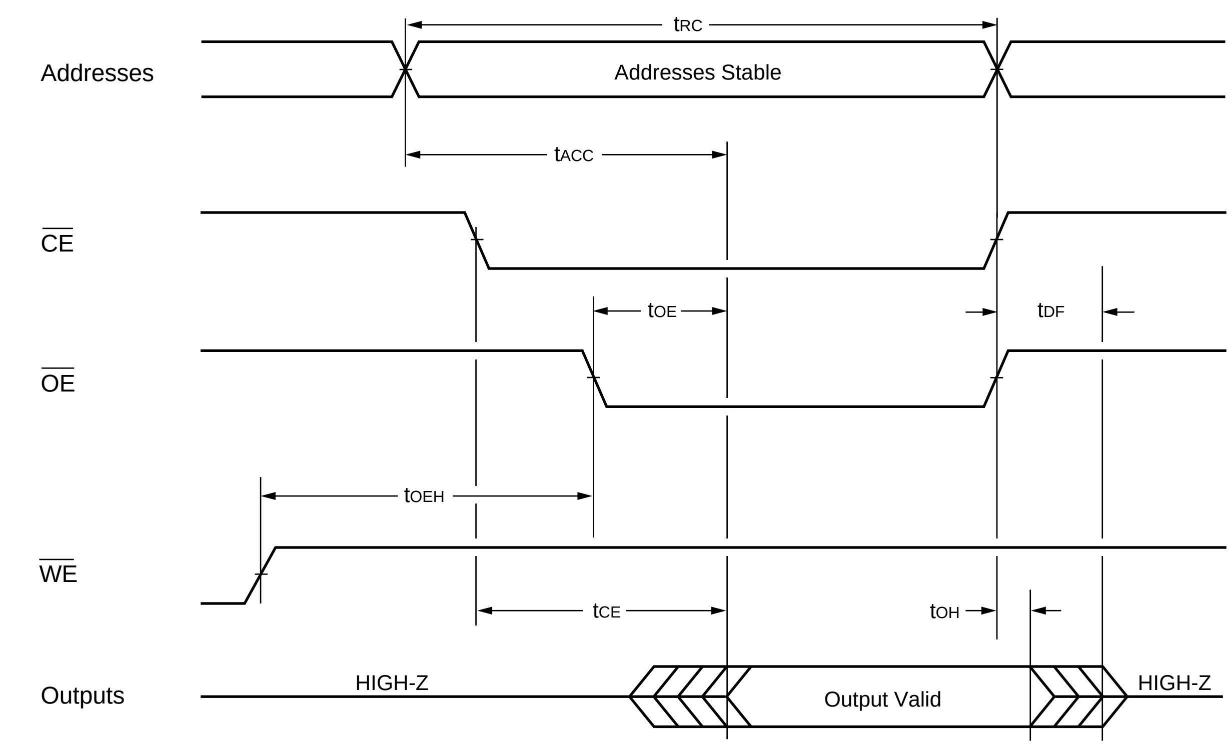


Figure 5.1 Read Operation Timing Diagram

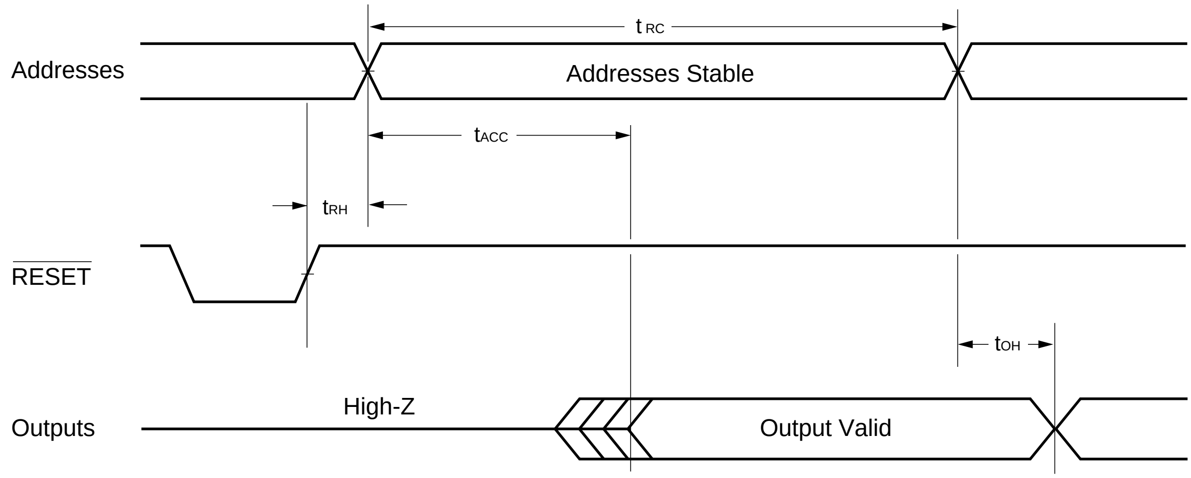
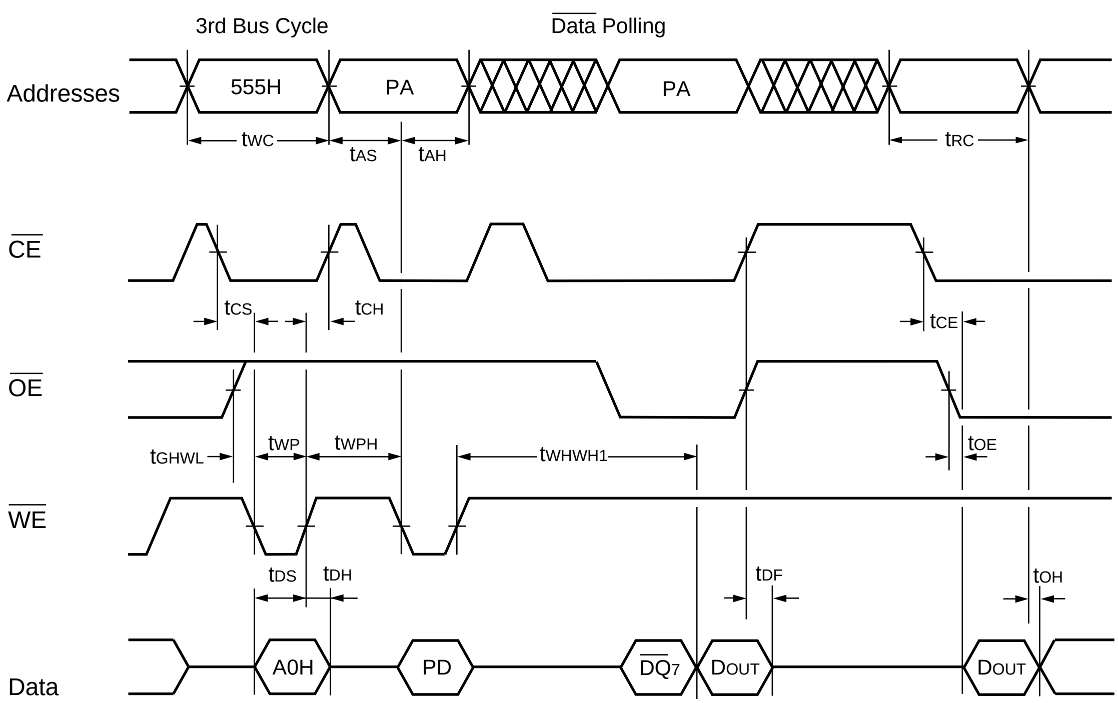
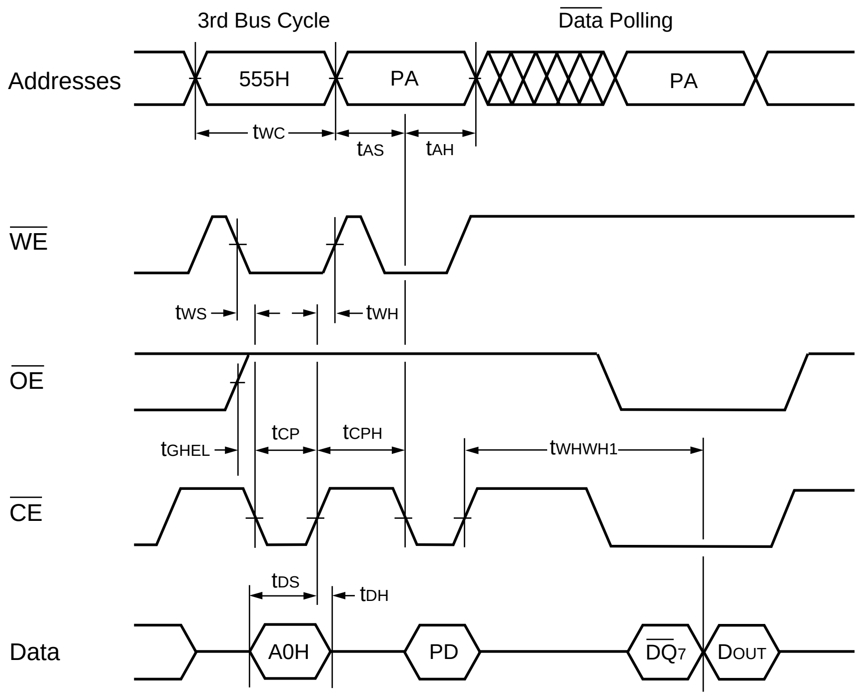


Figure 5.2 Hardware Reset/Read Operation Timing Diagram



Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at word address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 6 Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram



Notes: 1. PA is address of the memory location to be programmed.

2. PD is data to be programmed at word address.

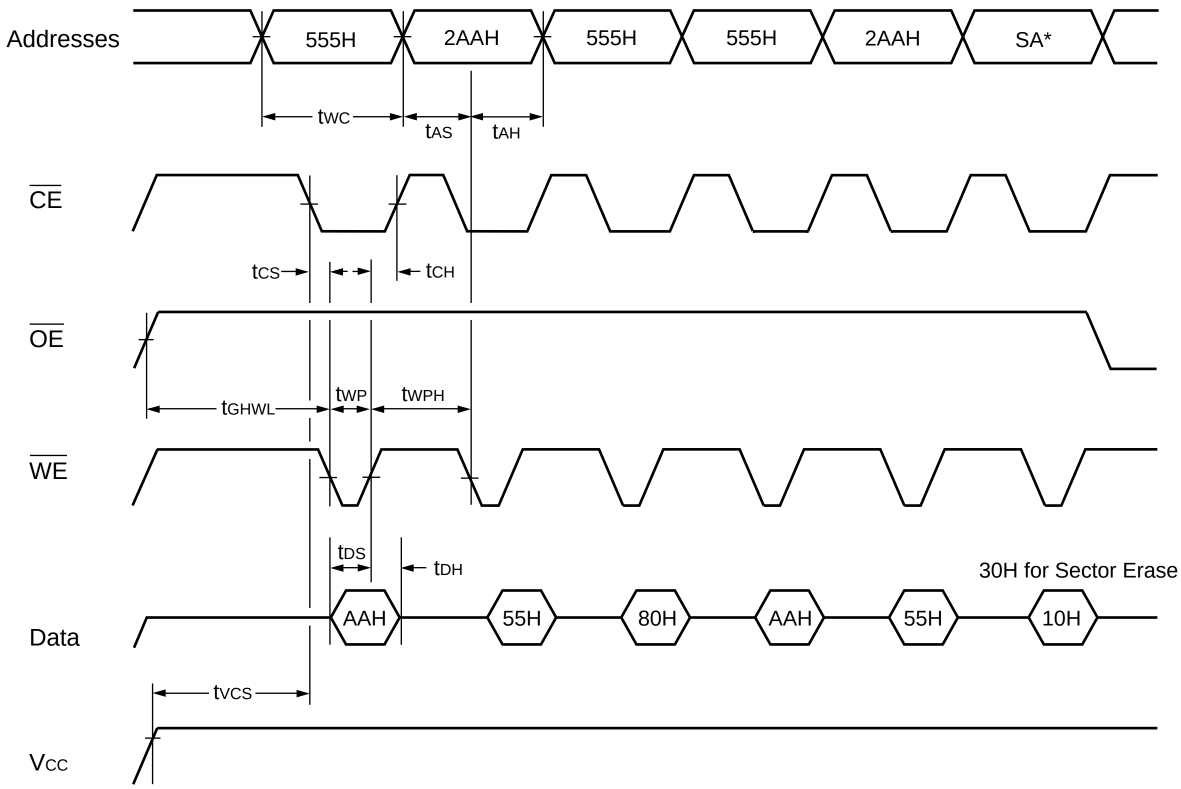
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.

4. D_{OUT} is the output of the data written to the device.

5. Figure indicates last two bus cycles out of four bus cycle sequence.

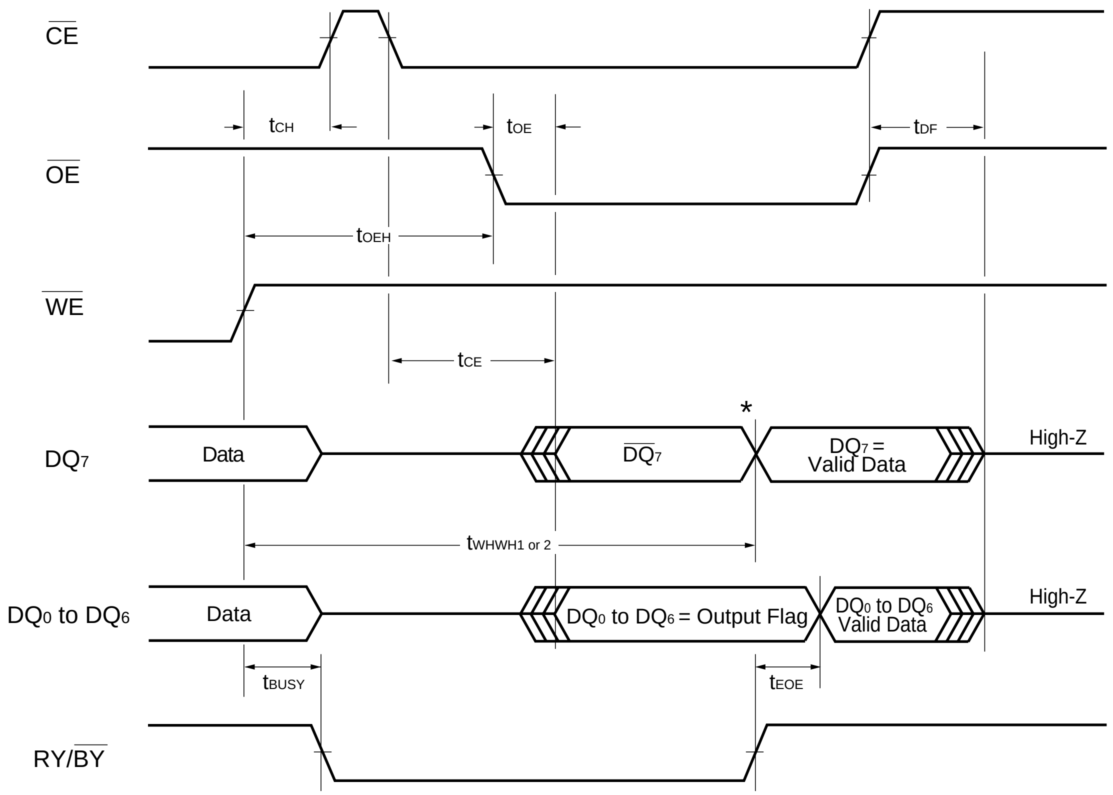
6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 7 Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram



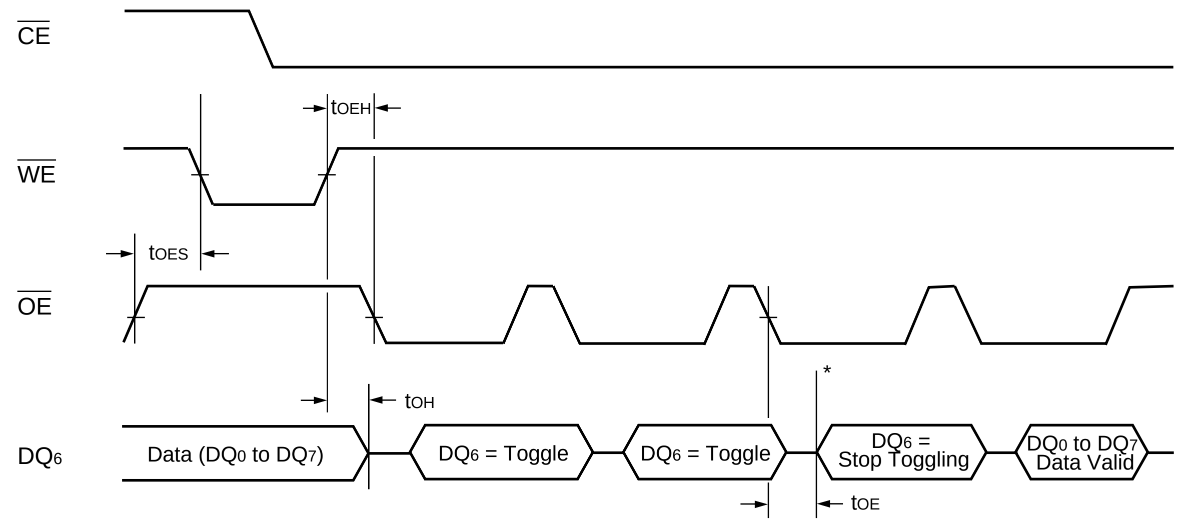
* : 1. SA is the sector address for Sector Erase. Addresses = 555H (Word), AAAH (Byte) for Chip Erase.
2. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 8 Chip/Sector Erase Operation Timing Diagram



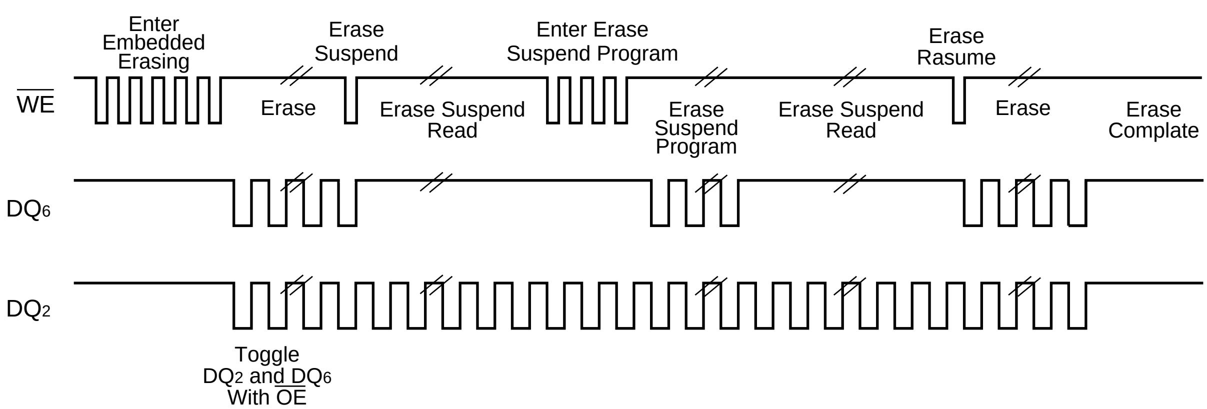
* : DQ_7 = Valid Data (The device has completed the Embedded operation).

Figure 9 $\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram



* : DQ_6 = Stops toggling. (The device has completed the Embedded operation.)

Figure 10 Taggle Bit I during Embedded Algorithm Operation Timing Diagram



Note: DQ_2 is read from the erase-suspended sector.

Figure 11 DQ_2 vs. DQ_6

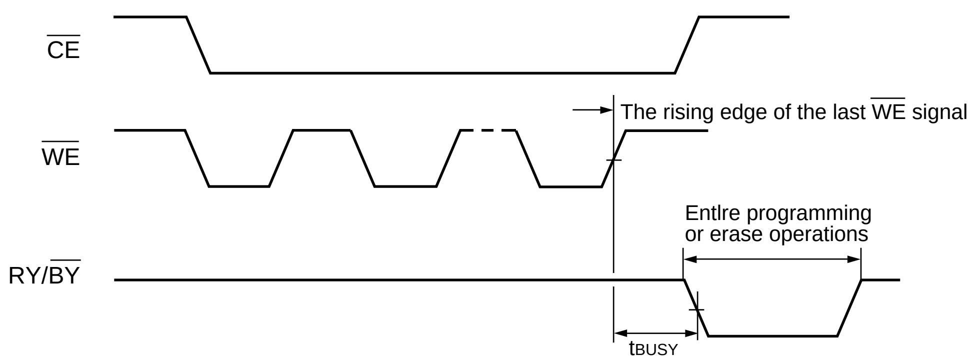


Figure 12 RY/BY Timing Diagram during Program/Erase Operation Timing Diagram

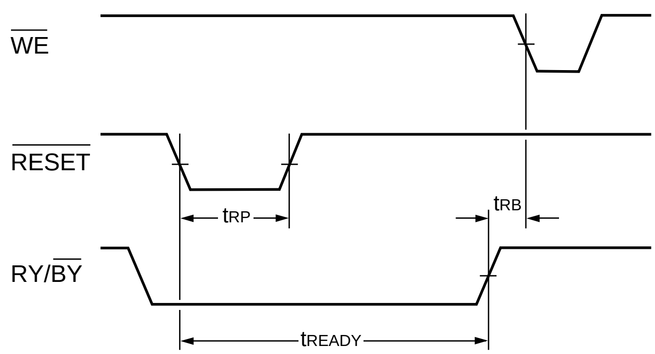


Figure 13 RESET, RY/BY Timing Diagram

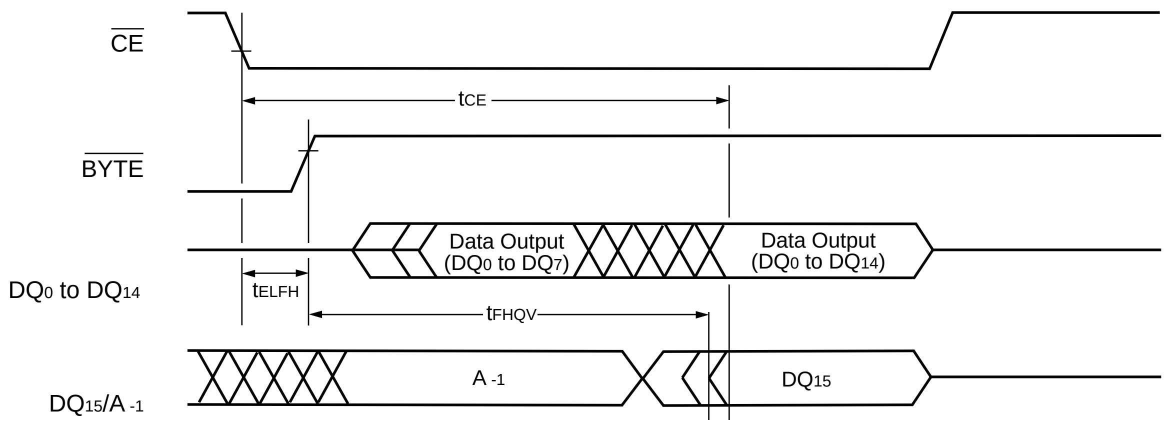


Figure 14 Timing Diagram for Word Mode Configuration

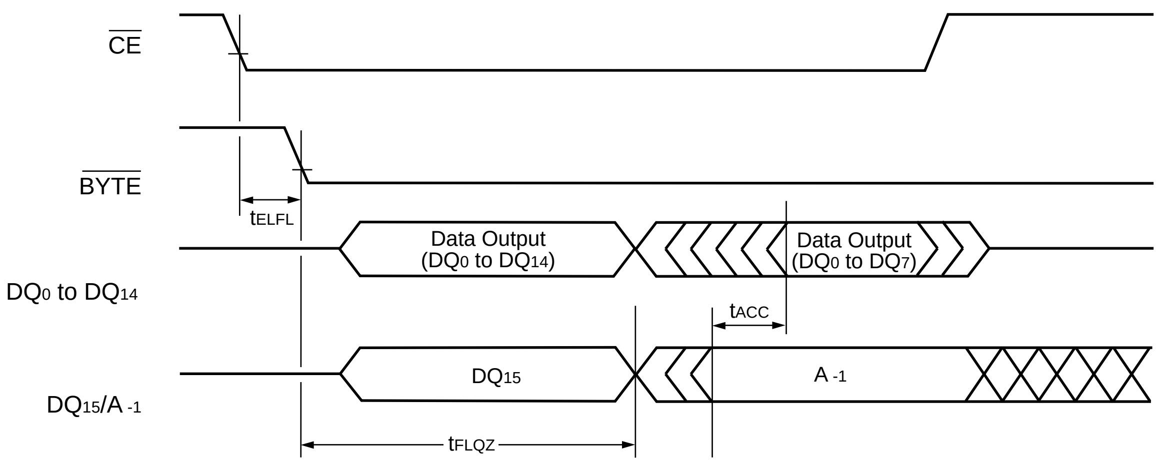


Figure 15 Timing Diagram for Byte Mode Configuration

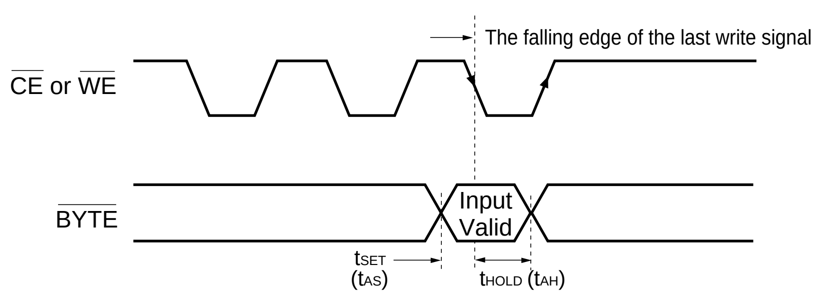
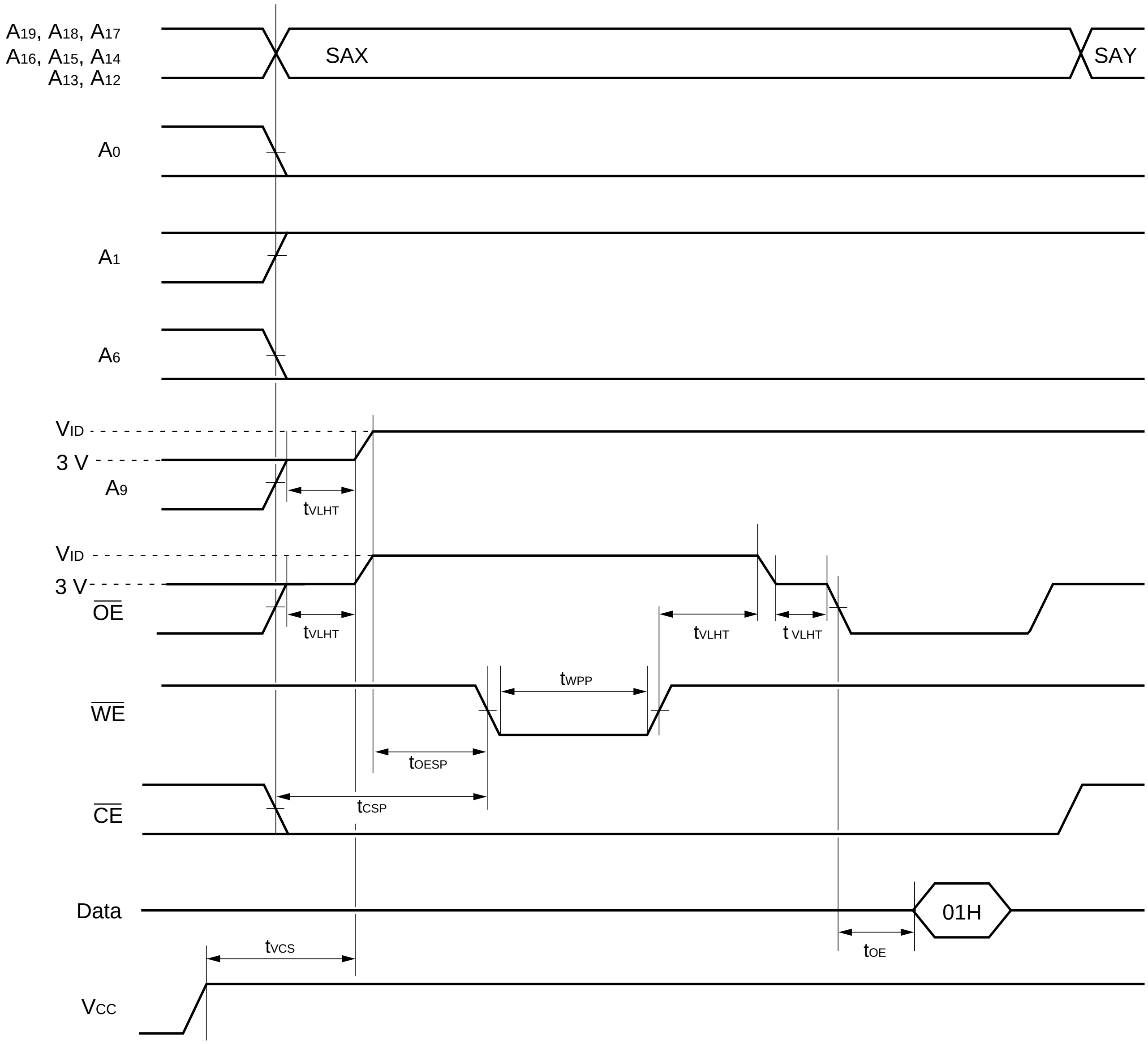


Figure 16 $\overline{\text{BYTE}}$ Timing Diagram for Write Operations



SAX : Sector Address for initial sector
SAY : Sector Address for next sector
Note: A_{-1} is V_{IL} on byte mode.

Figure 17 Sector Protection Timing Diagram

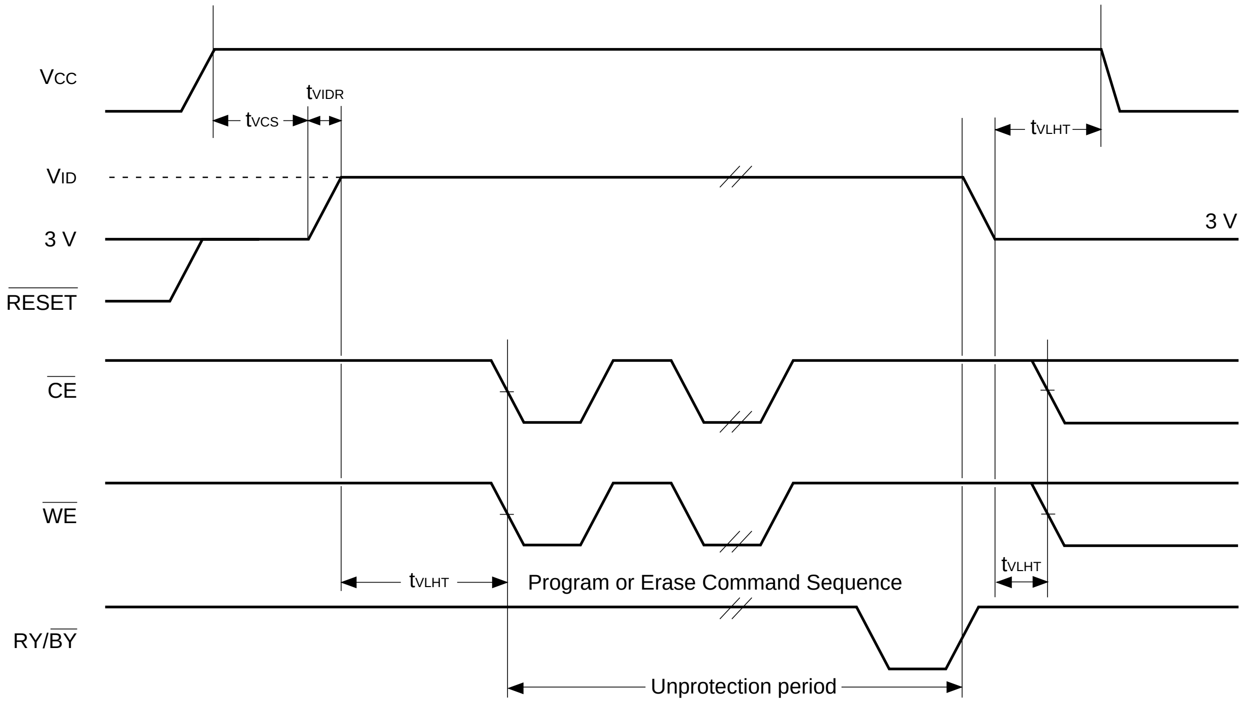
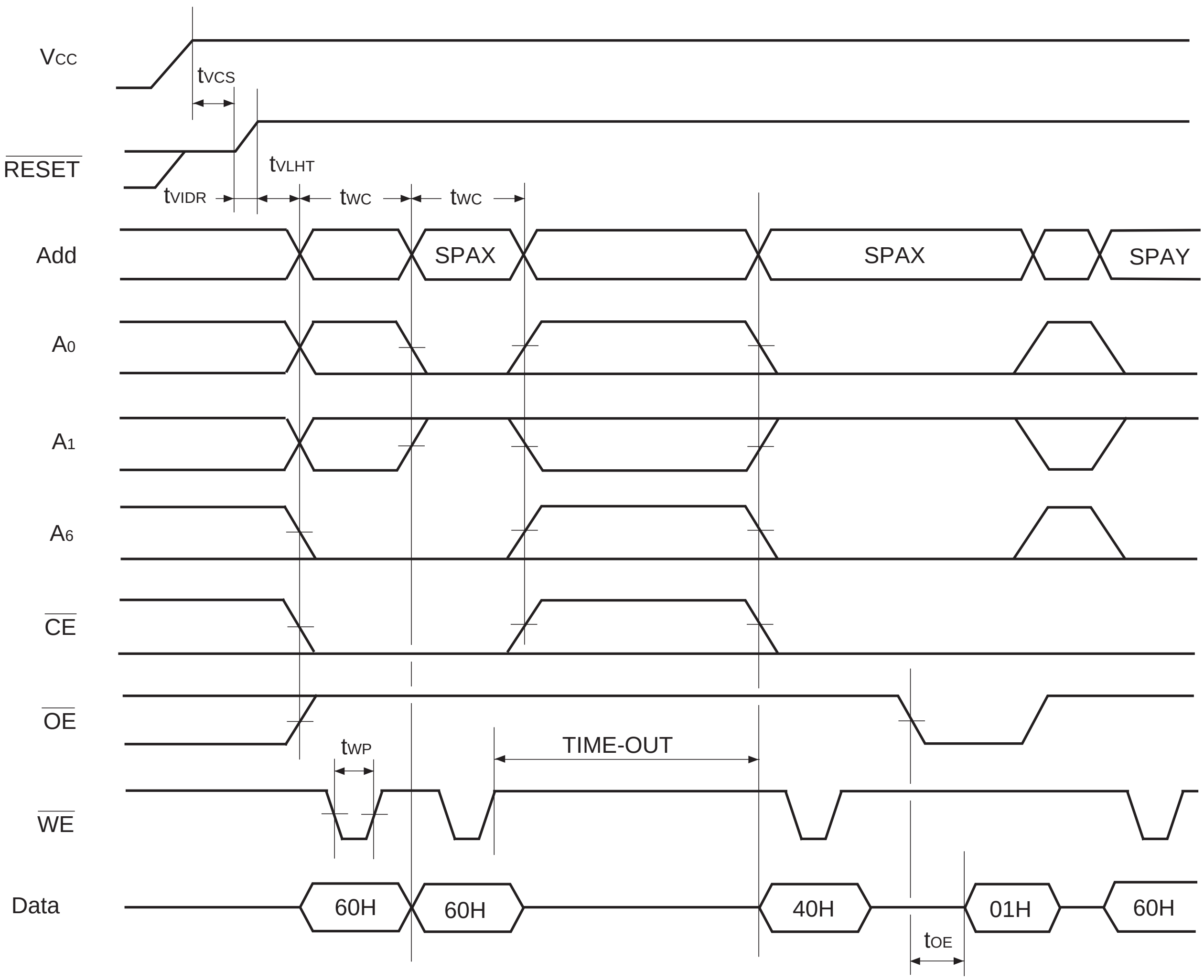


Figure 18 Temporary Sector Unprotection Timing Diagram

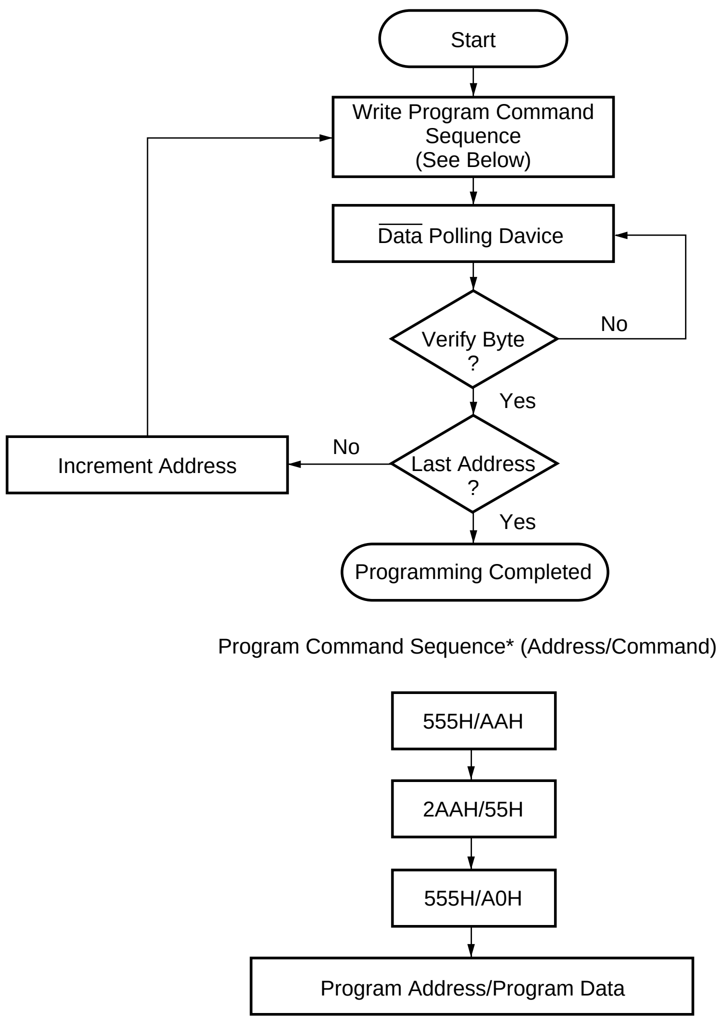


SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 250 µs (min)

Figure 19 Extended Sector Protection Timing Diagram

■ FLOW CHART

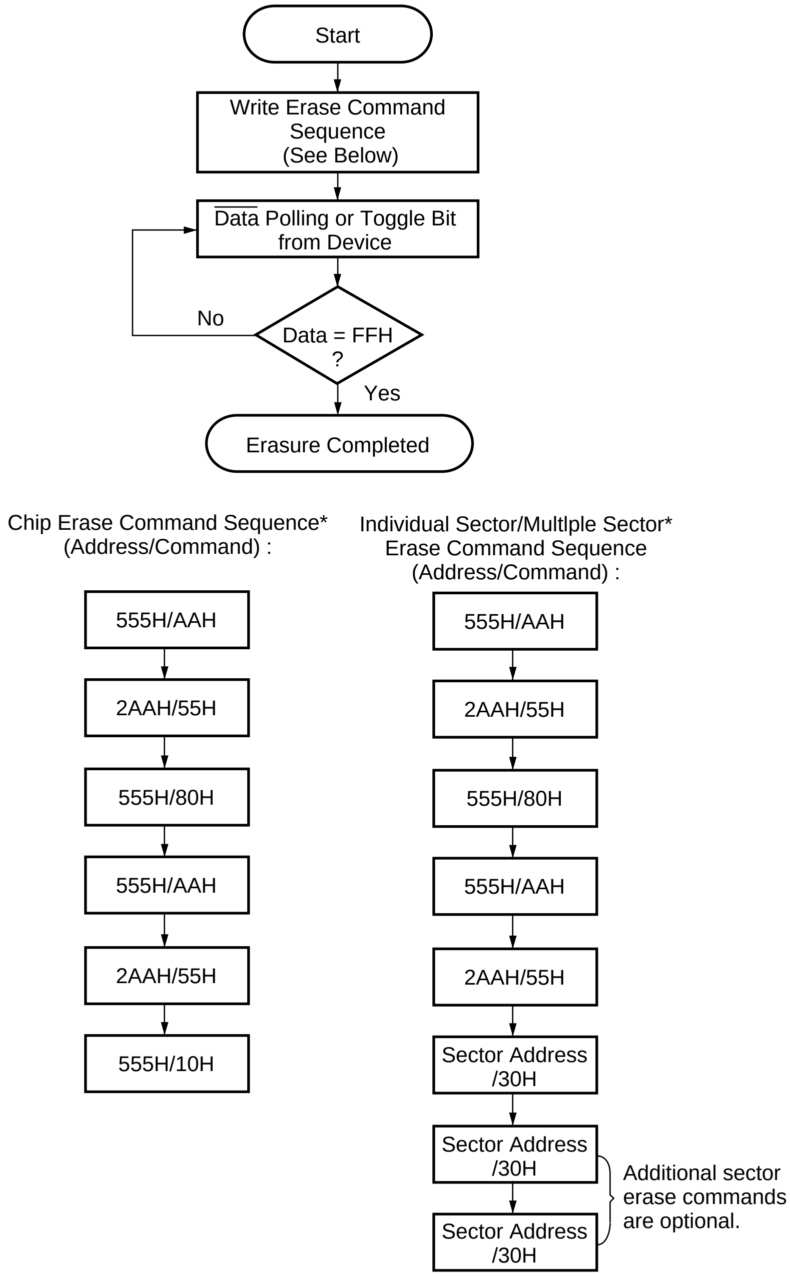
EMBEDDED ALGORITHM



* : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

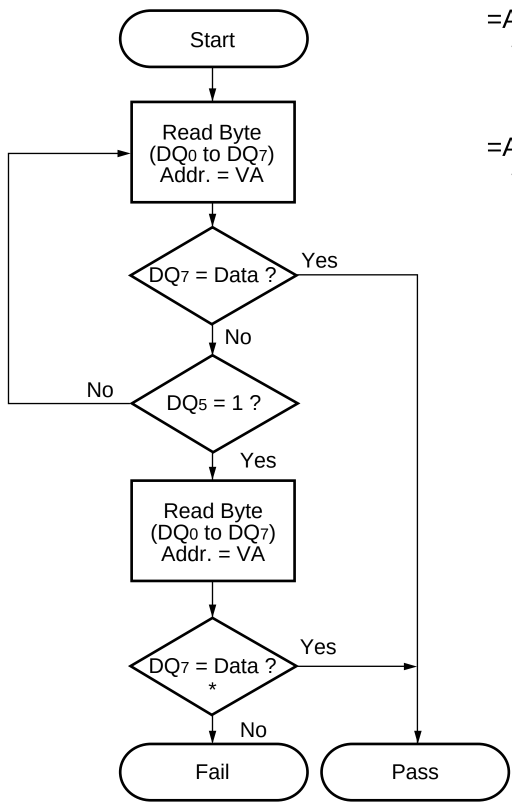
Figure 20 Embedded Program™ Algorithm

EMBEDDED ALGORITHM



* : The sequence is applied for ×16 mode.
The addresses differ from ×8 mode.

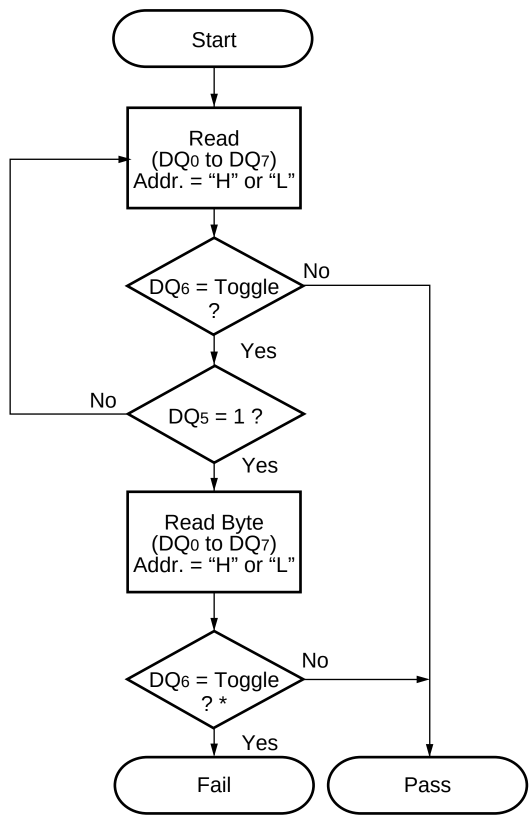
Figure 21 Embedded Erase™ Algorithm



VA =Address for programming
=Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.
=Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation.

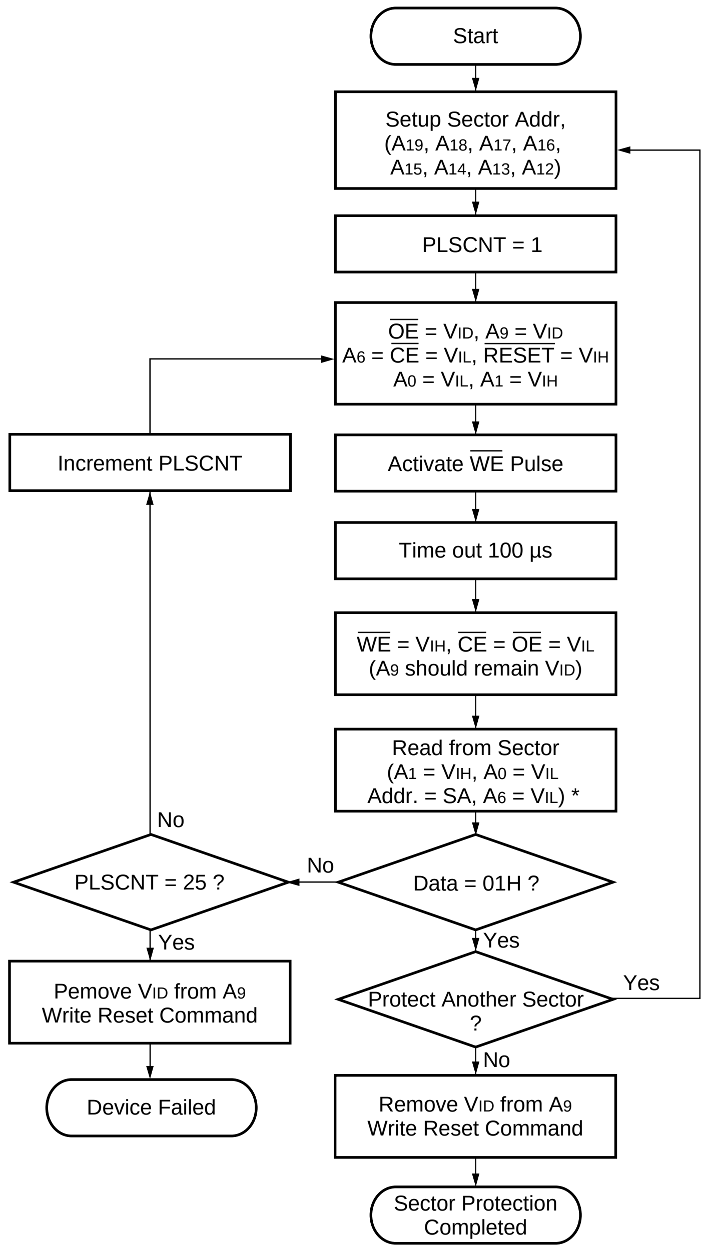
* : DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

Figure 22 $\overline{\text{Data}}$ Polling Algorithm



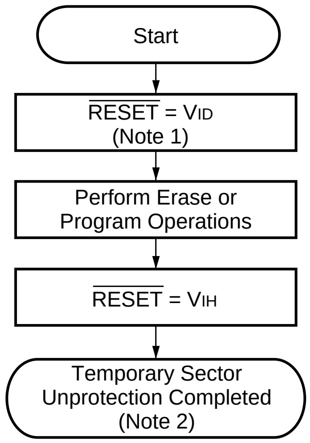
* : DQ_6 is rechecked even if DQ_5 = “1” because DQ_6 may stop toggling at the same time as DQ_5 changing to “1”.

Figure 23 Toggle Bit Algorithm



* : A_{-1} is V_{IL} on byte mode.

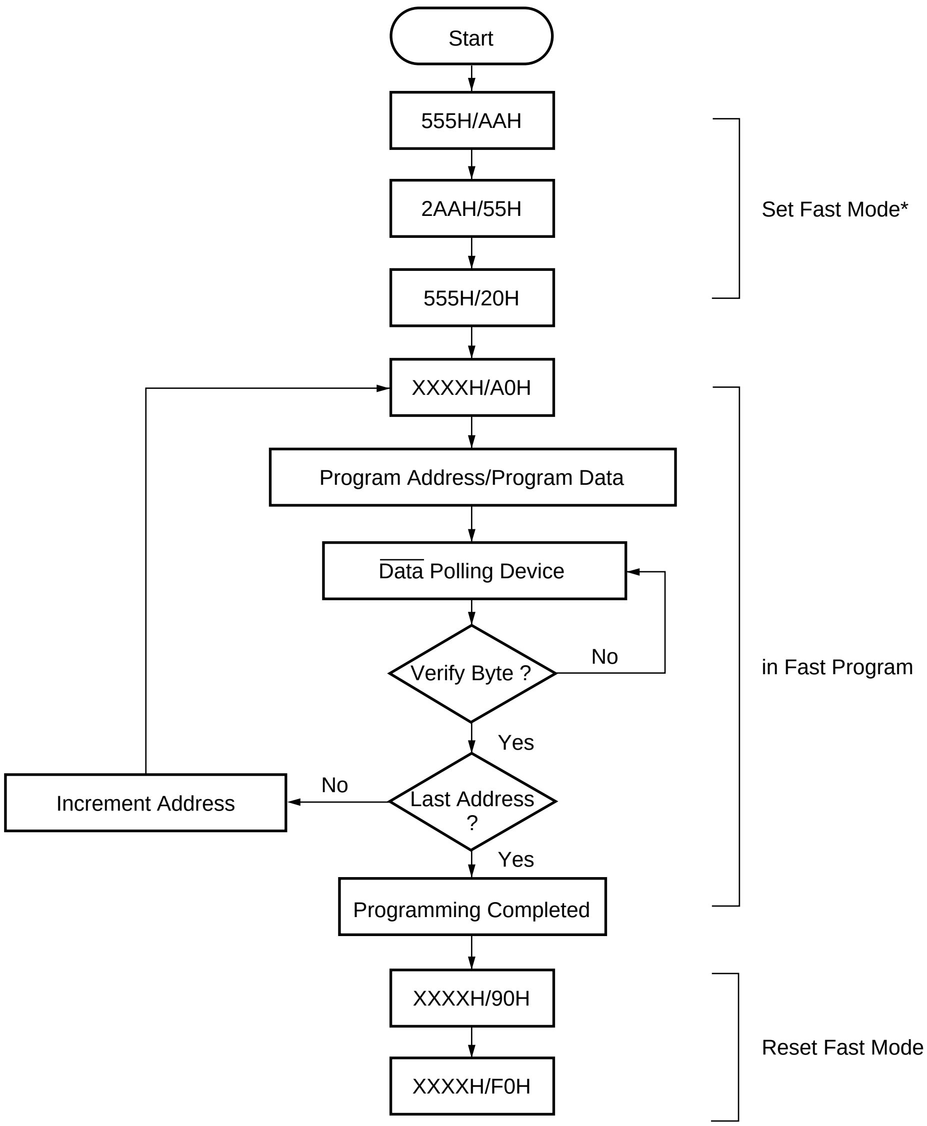
Figure 24 Sector Protection Algorithm



Notes: 1. All protected sectors are unprotected.
2. All previously protected sectors are protected once again.

Figure 25 Temporary Sector Unprotection Algorithm

FAST MODE ALGORITHM



* : The sequence is applied for ×16 mode.
* : The addresses differ from ×8 mode.

Figure 26 Embedded Programming Algorithm for Fast Mode

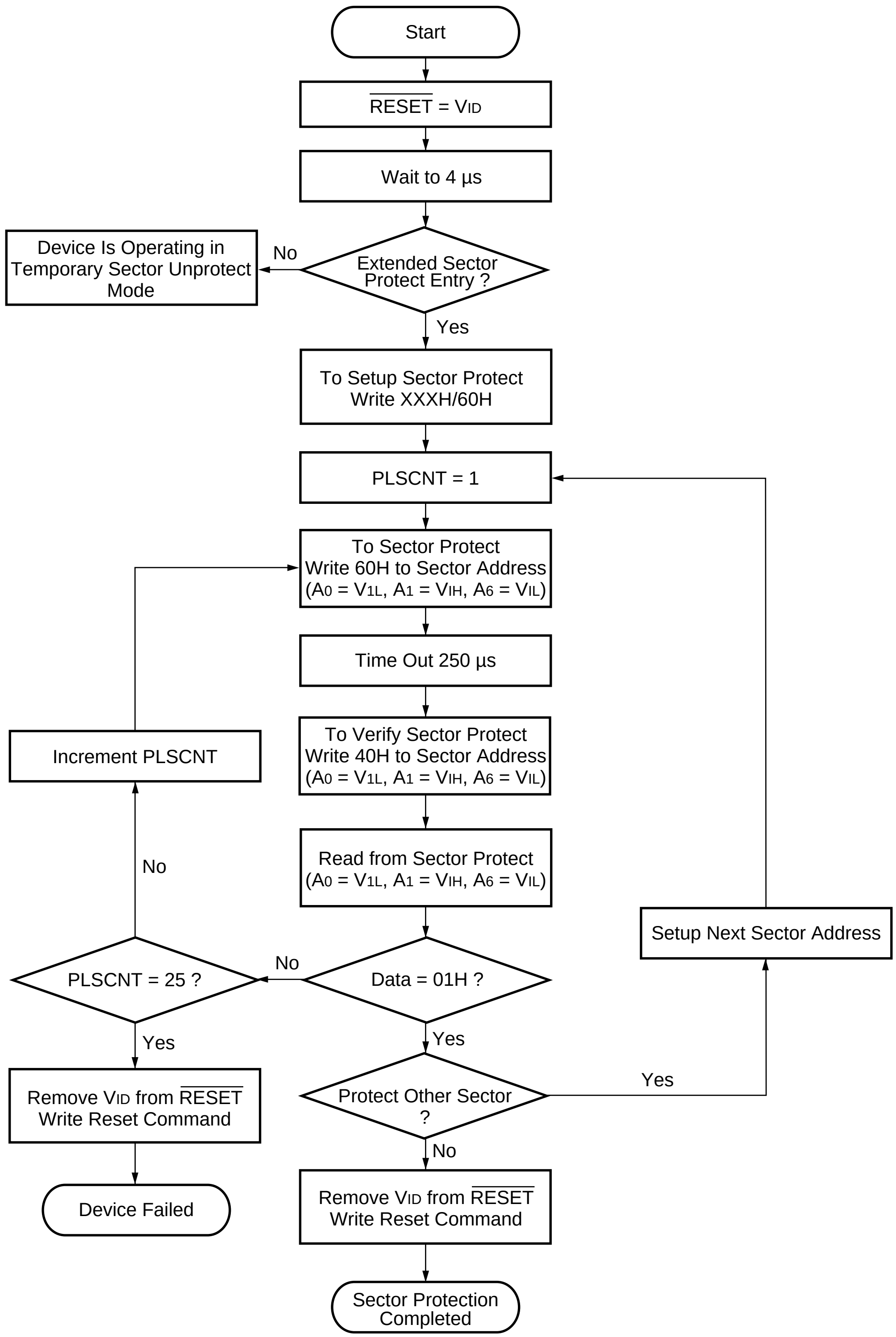


Figure 27 Extended Sector Protection Algorithm

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of:

MBM29LV160 T E 70 TN

PACKAGE TYPE (TN)
TN = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout
TR = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout
PCV = 48-Pin C- leaded Small Outline Package (CSOP)
PBT = 48-Pin Fine Pitch Ball Grid Array Package (FBGA)

SPEED OPTION (70)
See Product Selector Guide

DEVICE REVISION (E)

BOOT CODE SECTOR ARCHITECTURE (T)
T = Top sector
B = Bottom sector

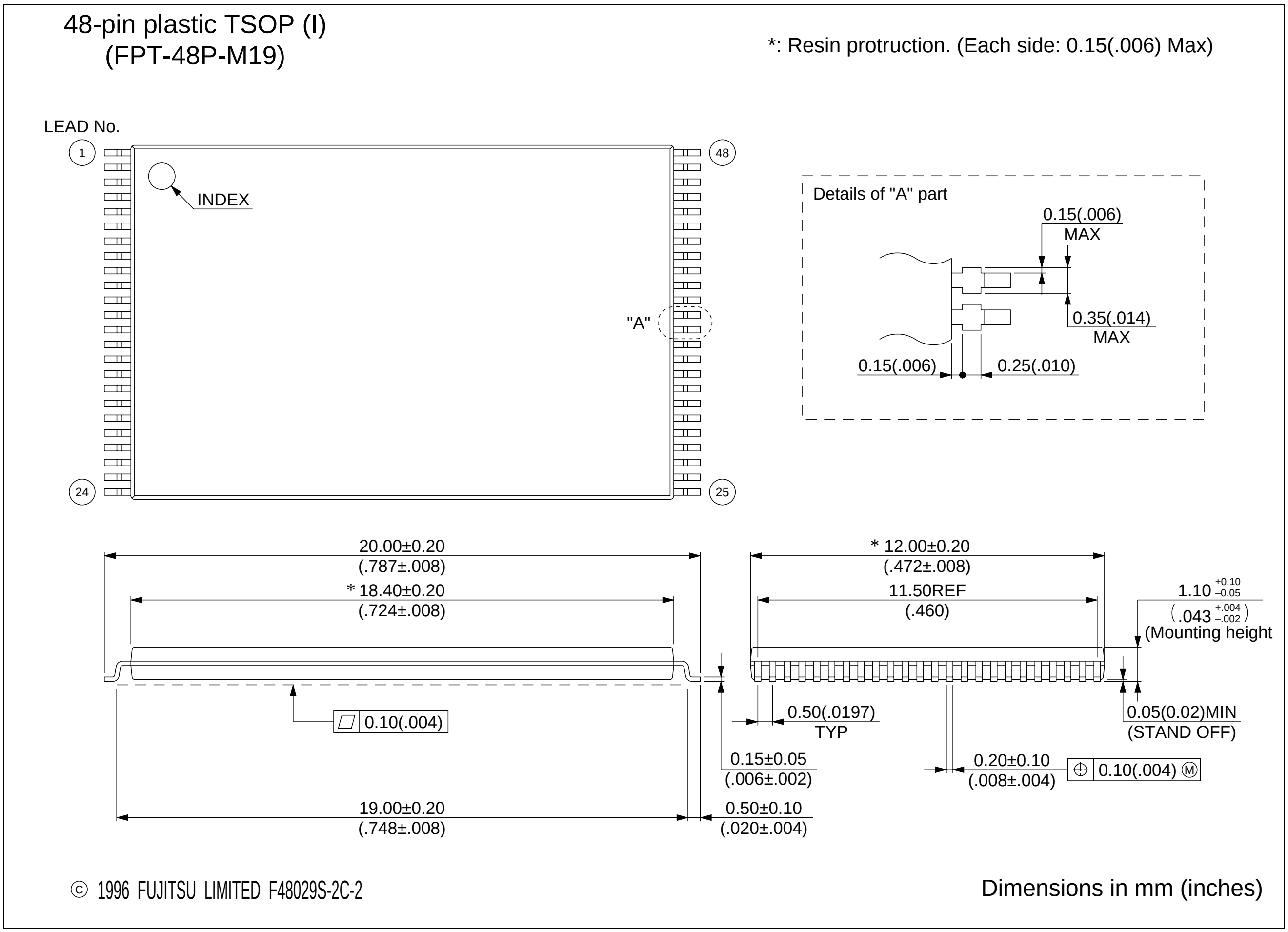
DEVICE NUMBER/DESCRIPTION (MBM29LV160)
MBM29LV160
16 Mega-bit (2M × 8-Bit or 1M × 16-Bit) CMOS Flash Memory
3.0 V-only Read, Write, and Erase

Valid Combinations		
MBM29LV160TE/BE	70 90 12	TN TR PCV PBT

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

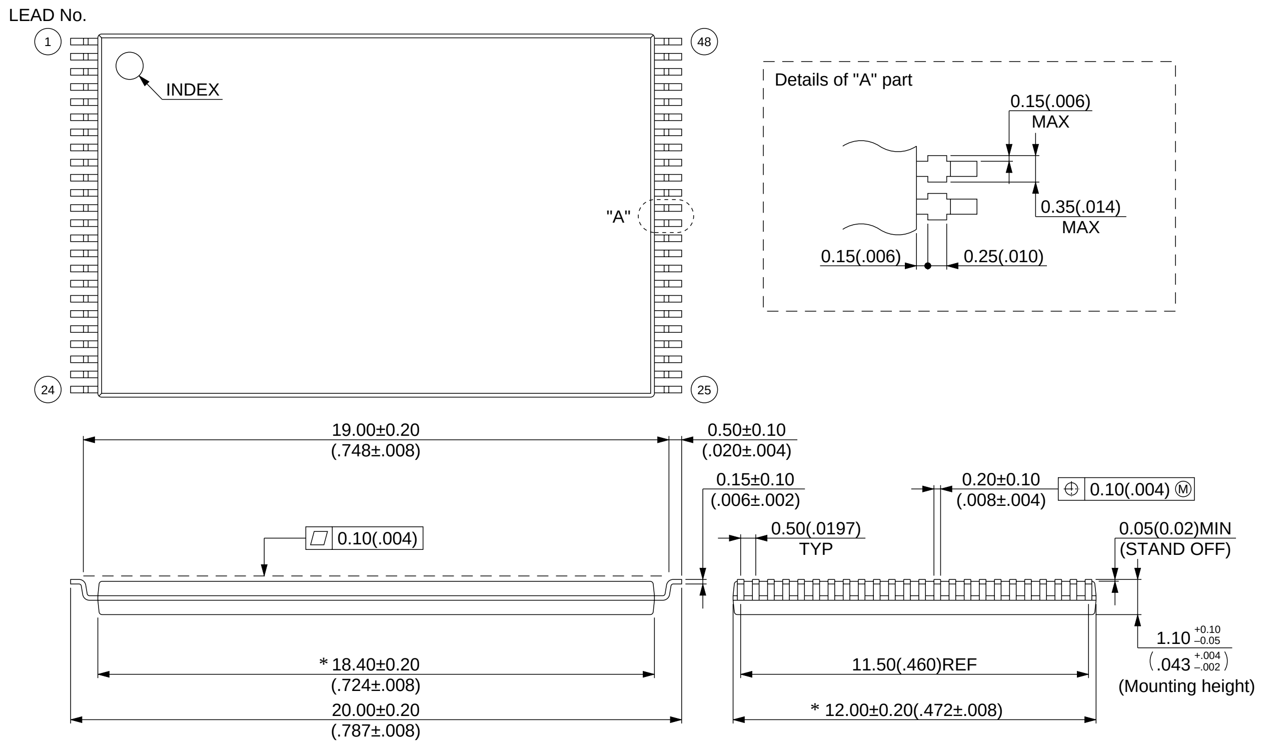
■ PACKAGE DIMENSIONS



(Continued)

48-pin plastic TSOP (I)
(FPT-48P-M20)

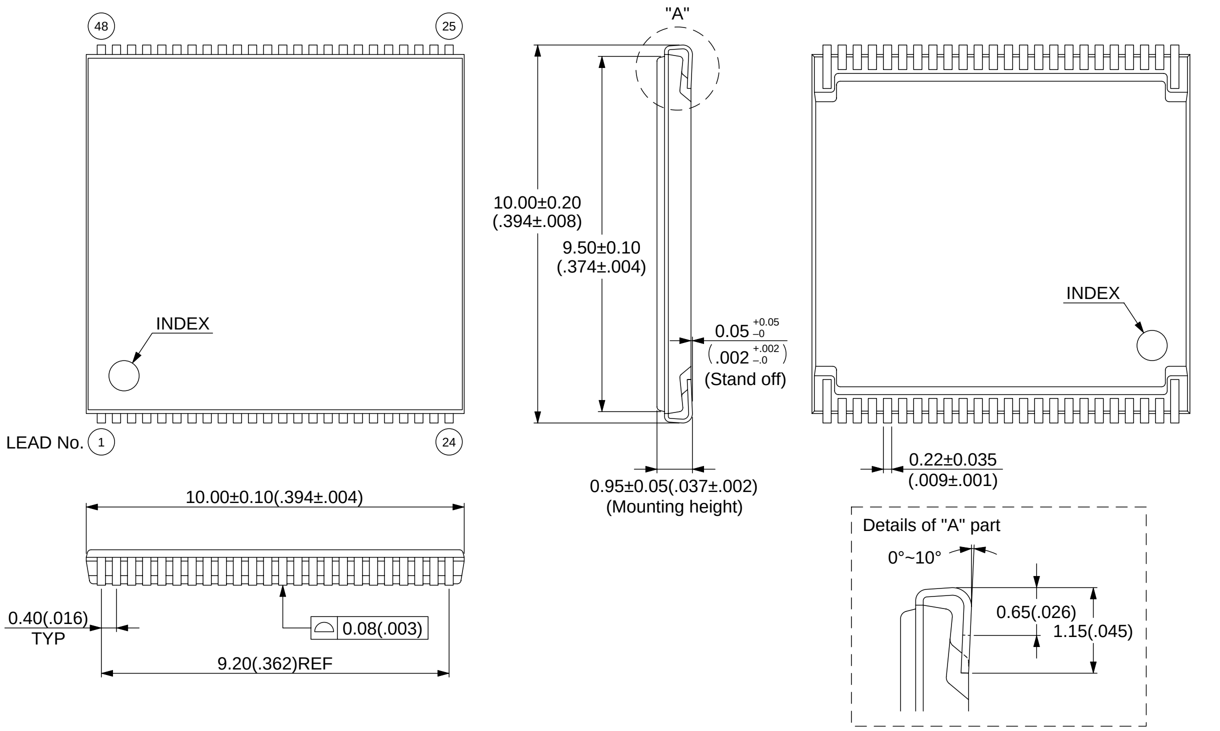
*: Resin protrusion. (Each side: 0.15(.006) Max)



Dimensions in mm (inches)

(Continued)

48-pin plastic CSOP
(LCC-48P-M03)



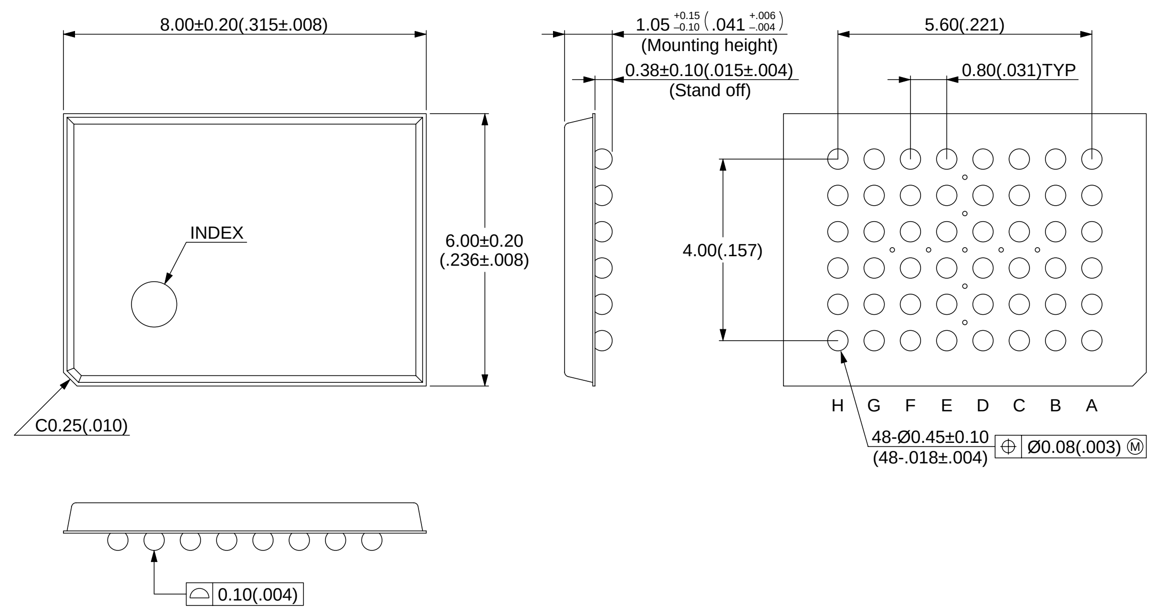
Dimensions in mm (inches)

(Continued)

(Continued)

48-pin plastic FBGA
(BGA-48P-M11)

Note: The actual shape of corners may differ from the dimension.



Dimensions in mm (inches)

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